Solid-State Electronics 60 (2011) 116–121

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions

B. Vincent [a,*], R. Loo [a], W. Vandervorst [a,b], J. Delmotte [a], B. Douhard [a], V.K. Valev [c], M. Vanbel [c], T. Verbiest [c], J. Rip [a], B. Brijs [a], T. Conard [a], C. Claypool [d], S. Takeuchi [e,1], S. Zaima [e], J. Mitard [a], B. De Jaeger [a], J. Dekoster [a], M. Caymax [a]

[a] IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[b] Instituut voor Kern-en Stralingsfysica, K.U. Leuven, Leuven, Belgium
[c] Molecular and Nanomaterials, K.U. Leuven, Leuven, Belgium
[d] Scientific Computing International, Carlsbad, CA, USA
[e] Department of Crystalline Materials Science, Nagoya University, Nagoya, Japan

ARTICLE INFO

*Article history:*
Available online 3 March 2011

*Keywords:*
Germanium MOSFET
Germanium passivation
Ultrathin Si growth on germanium
Si precursors
Low temperature CVD
Trisilane

ABSTRACT

Ultra thin Si cap growth by Reduced Pressure Chemical Vapor Deposition on relaxed Ge substrates is detailed in this paper for Ge pMOSFET (Metal Oxide Semiconductor Field Effect Transistors) passivation purposes. A cross calibration of different measurement techniques is first proposed to perfectly monitor Si monolayers thickness deposited on Ge substrates. Different characteristics, impacting Ge pMOSFETs device performances, are next detailed for various Si cap growth processes using different Si precursors: DiChloroSilane (DCS), silane and trisilane. The critical Si thickness of plastic relaxation has been determined at 12 monolayers. Presence of point defects has been identified for very low growth temperature as 350 °C. Ge–Si intermixing, caused by a Ge segregation mechanism, is strongly reduced by the use of trisilane as Si precursor at low temperatures.



## 1. Introduction

Passivation of high mobility materials is today considered as the main challenge for replacement of silicon in MOSFETs channels for beyond 22 nm technology nodes [1]. For pMOSFETs, germanium is identified as a particular good candidate [2] and many passivation routes have been proposed by introducing different Ge-high K interlayers: $GeO_2$ [3], GeON [4], S [5], Sr [6] and ultrathin Si cap [7–9]. The latter passivation scheme permits to introduce Si back into Ge MOSFET processing as a well-known starting surface for high K-metal gate stack deposition.

Ge pMOSFET performances with Si passivation have been reported frequently in literature during the last years [10–12]. Si cap monolayers thickness and Si cap growth process have been highlighted to impact severely device performances, as hole mobility, Density of Interface Traps ($D_{IT}$), and Capacitance Equivalent Thickness (CET). So far, we have investigated two Si growth processes using silane at 500 °C and trisilane at 350 °C, respectively as Si precursor. For each process, an optimal Si monolayer thickness has been defined providing an ultimate hole mobility peak value [10]. Trisilane has the benefit to lower $D_{IT}$ and CET values whereas it does not allow to reach as high hole mobility values as the ones obtained with silane. Depending on the growth conditions, Si cap on Ge presents then different characteristics which directly impact device performances.

This paper focuses on characterization of ultrathin Si layers grown on Ge substrates by Reduced Pressure Chemical Vapor Deposition (RPCVD). In a first section, thickness measurement of few monolayers thin Si cap is discussed and characterization techniques are detailed. In the second section, different properties of Si cap layers will be analyzed: strain relaxation, Ge segregation in Si cap and point defects formation.

## 2. Samples preparation and characterization techniques

### 2.1. Samples preparation

The ultra thin epitaxial strained Si layers have been grown in a ASM Epsilon RPCVD equipment on blanket 200 mm Ge virtual substrates. Ge virtual substrates have been obtained by growing previously 1 μm thick relaxed Ge layers on Si substrates followed by a Chemico Mechanical Planarization (CMP) to obtain smooth Ge starting surfaces (rms roughness = 0.2–0.4 nm, $Z_{max}$ = 5 nm) [13]. Ge (300 nm) is typically removed by CMP. Before Si cap growth, the 700 nm Ge/Si layers have received an HF clean and a $H_2$ bake at 650 °C.

* Corresponding author.
*E-mail address:* benjamin.vincent@imec.be (B. Vincent).
[1] Present address: Covalent Silicon Co. Ltd., Higashikou, Japan.

0038-1101/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2011.01.049

Different Si precursors have been used for Si cap growth: DiChloroSilane (DCS), silane and trisilane. Each precursor has a minimal temperature at which Si can be grown as detailed in [14]: 650 °C for DCS, 500 °C for silane, 350 °C for trisilane, respectively. Only low Si cap growth temperatures have been investigated in order to avoid Ge thermal up-diffusion in Si caps. From [15], no thermal diffusion of Ge in strained Si is expected for temperatures below 700 °C. After Si cap growth, wafers are ramped from growth temperatures down to 200 °C under $H_2$ and are unloaded. The H coverage layer formed during the temperature ramp down permits to avoid direct re-oxidation of the Si cap layers during unloading and air exposure.

### 2.2. Ultrathin Si cap thickness measurement on Ge

Si cap layers grown on Ge require being very thin in order to avoid Si strain relaxation and associated defects creation. Critical thickness of plastic relaxation was recently determined in the 6–12MLs range from [7].

Since the quantity of monolayers deposited has a severe impact on electrical performances [11], a reliable measurement technique is mandatory to control perfectly the Si thicknesses deposited. Different techniques are proposed in this section to measure the amount of Si on Ge surfaces: Rutherford Back Scattering (RBS), Total X-Ray Fluorescence (TXRF), X-ray Photoelectron Spectroscopy (XPS), Spectroscopic Ellipsometry (SE), and a combined multiple-angle reflectometry and grazing angle Spectroscopic Ellipsometry technique (FilmTek 4000EM-DUV), detailed in [16].

SE measurements have been performed right after unloading the samples from the reactor. The SE fitting model used consists of a $SiO_2$/Si/Ge stack on Si substrate. The native oxide is always fitted as a non-existing layer when the measurement is done directly after unloading as the native oxide starts to be formed only after a few minutes of air exposure. The Si thickness fitted in nm by SE is converted in monolayers taking into account 1ML = 0.13125 nm.

The other measurements have been done a few hours up to a few days after the growth, taking then into account the existence of a native oxide on the Si caps. The total quantity of Si deposited (present now as native oxide and a remaining Si cap) was measured by RBS or TXRF, and converted in number of monolayers taking into account 1ML = 6.2485e14 at/cm$^2$ (Ge atomic density). The combined Reflectometry–Ellipsometry technique, which consists of simultaneous reflection measurements at normal to the surface (0°) and oblique (70°) angles, along with the phase ($\Delta$) and amplitude ratio ($\Psi$) values obtained from grazing angle ellipsometric measurements, permits the determination of the total quantity of Si deposited on Ge by fitting the native oxide/remaining Si bilayer as an equivalent unique Si layer deposited on Ge and having the same Si quantity. XPS permits to determine separately the native oxide thickness, $t_{SiO2}$, and the remaining Si cap one, $t_{Si}^{rem}$ The corresponding Si deposited thickness, $t_{Si}^{dep}$, is then calculated by:

$$t_{Si}^{dep} = t_{Si}^{rem} + (t_{SiO2}/2.25) \quad (1)$$

RBS has the benefit to provide the absolute quantity of Si present on Ge surface by integrating the Si spectrum of interest. However, specific Ge thicknesses are required to avoid the overlap of the Ge and the Si spectra; 200 nm thick Ge layers on Si were obtained with longer CMP. On these samples two distinct spectra (as shown in Fig. 1) related to a few Si monolayers can be obtained using a He+beam, 1.02 MeV energy and 170° scatter angle. For thicker Ge underlayers, the Si RBS signal is not distinguishable from the Ge one.

Two different TXRF detectors (respectively named Rigaku and Atomika detectors) have then been calibrated with RBS by growing different Si caps on 200 nm Ge CMPed substrates. The detectors

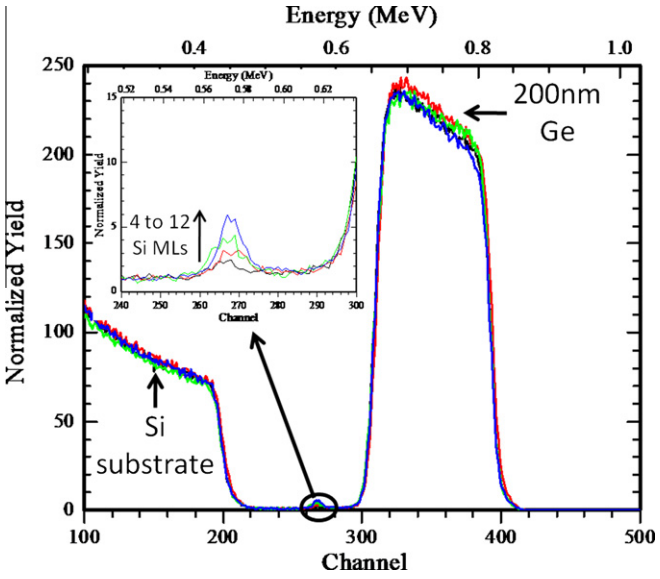


**Fig. 1.** Rutherford Back Scattering spectra of 4–12MLs Si grown on 200 nm CMPed Ge/Si substrates. Separation of Si and Ge spectra permits to determine the quantity of Si monolayers deposited on Ge.

were previously cross calibrated using Ni droplets on Si substrates and Ni concentration measurements. Fig. 2 shows the comparison of the TXRF measurements with respect to absolute RBS measurement: a 1.26 correction factor is determined for TXRF detection of Si atoms on Ge surfaces. With correction, TXRF has then been configured as a reference technique to measure Si cap grown on any kind of Ge substrates (bulk Ge or thicker Ge/Si substrates).

XPS, SE and combined Reflectometry–Ellipsometry techniques have further been calibrated to the corrected TXRF measurements. Fig. 3 compares measurements for 2–10 MLs thick Si caps grown on Ge bulk or on 700 nm Ge blanket substrates with different growth processes. We note an overestimation of Si thickness as determined by XPS by a factor of 1.4 which is close to the uncertainty factor of the Si XPS cross section. Both ellipsometric

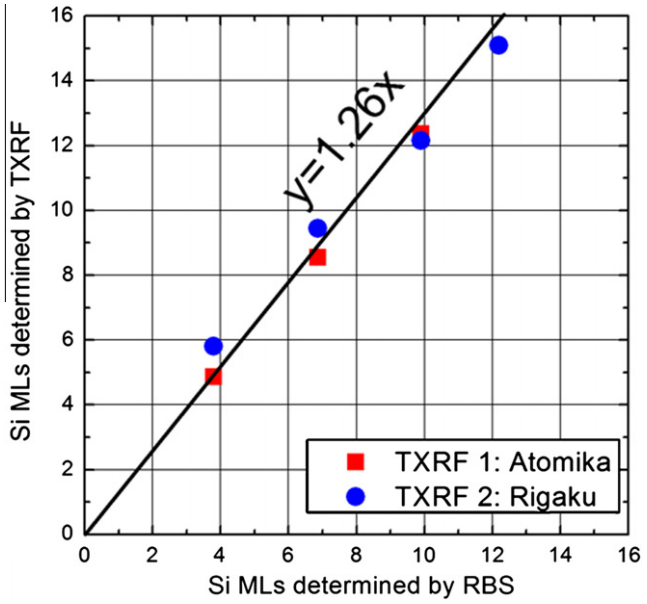


**Fig. 2.** Total X-Ray Fluorescence calibration with RBS on samples from Fig. 1 using two different TXRF detectors. A 1.26 correction factor is determined for TXRF measurements of 4–12MLs Si layers grown on Ge.

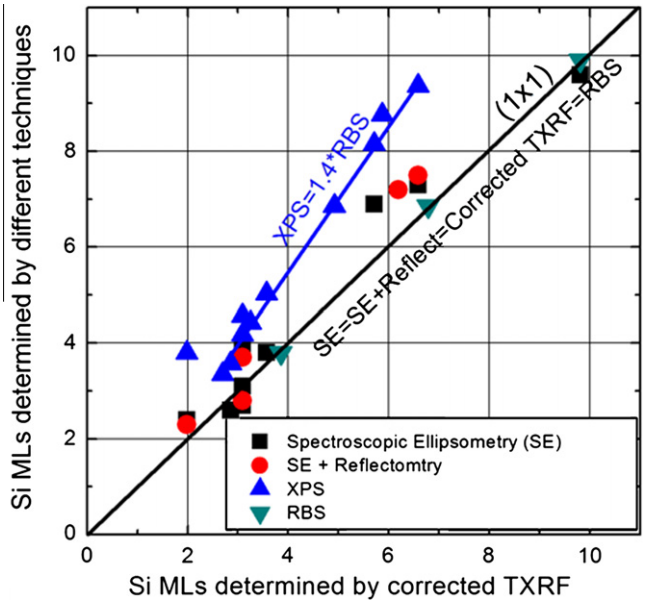


**Fig. 3.** Cross calibration of XPS, Spectroscopic Ellipsometry and combined Reflectometry–Ellipsometry (FilmTek 4000EM-DUV) with corrected TXRF from Fig. 2 on 2–10MLs Si cap grown on 700 nm Ge/Si CMPed substrates. XPS overestimates Si thickness by a factor of 1.4 and ellipsometric techniques correlate perfectly with TXRF measurement reference.

techniques present a very good correlation (±0.5MLs) as compared to corrected TXRF.

The previous cross calibration of measurement techniques has permitted to define reliable ways to monitor the Si thickness of few monolayers grown on Ge substrates. RBS gives the absolute Si amount present on Ge surface but requires specific thin Ge structures. TXRF, with correction, has thus been used as reference measurement for other techniques calibrations to measure Si thickness grown on different kind of Ge substrates. Whereas XPS needs a similar correction as TXRF, ellipsometric measurements correlate perfectly with corrected TXRF in the 2–10MLs Si cap thickness range. Ellipsometric measurements have moreover the benefit to be non-destructive and to allow measurement on pattern structures, as Ge structures in Shallow Trench Isolation (STI) for instance [17]. In the rest of the paper, all Si ML thicknesses specified have been measured by Spectroscopic Ellipsometry.

### 2.3. Characterization techniques

Mitard et al. reported recently that identical Si caps thicknesses being grown either with silane or trisilane as Si precursor on Ge pMOSFETs channels provide different device performances [11]. Not only the Si thickness but other properties linked to Si growth conditions need thus to be investigated in order to fully understand their impact on devices characteristics.

Extremely Low Energy SIMS (EXLE SIMS) [18] has been used to investigate Si–Ge intermixing at the Si cap/Ge layer interface. A very high depth resolution is necessary in this case since the Si caps are only few monolayers thick. Both transient region (artifact SIMS surface peak) and decay length (artifact SIMS tails) need to be reduced to determine the exact Ge slope in the Si cap without any overlapping of a Ge surface peak. These artifacts are reduced by decreasing the ion beam mixing with the help of very low sputter energies. In a recent work done on low energy SIMS sputtering on a Si/SiGe/Si bulk stack using a $O_2$ beam and 100 eV sputter energy, we achieved a Ge slope as steep as 1.2 nm/dec, which is the steepest profile ever recorded with our SIMS conditions. For characterization of the Si–Ge intermixing in the Si cap grown on the Ge substrates, the upslope is of relevance which is typically 1.5–2× smaller than the down slope, leading to an estimated resolution ~0.6–0.8 nm/dec @150 eV $O_2$ as used in the present experiments.

Second Harmonic Generation (SHG) has been used to characterize the quality of the epitaxial Si cap layers grown on Ge [19,20]. A Ti:Sapphire laser at 800 nm with a 150 fs pulse width and a 82Mz repetition rate has been used. A polarizer and a half wave plate are set up before the incident beam reaches the Si/Ge sample. The incidence angle is fixed to 45°. A low band pass filter/analyser/photomultiplier combination is used to detect the SH signal generated from the sample at 400 nm. The SHG response is recorded as function of the sample rotation angle, for a polarizer along the plane of incidence (S-polarized) and an analyzer along a direction perpendicular to the plane of incidence (P-polarized). In this polarizer–analyzer configuration, the non-linear response is characterized by a single tensor element. Upon recording the SHG response for a 360° rotation of the sample, this tensor element produces a squared sine function. Any materials symmetry modification due to presence of defects (point defects or relaxation defects) might impact the SH response of the layer.

Additionally, cross-sectional and plan view Transmission Electron Microscopy (TEM) have been performed to characterize the eventual dislocation formation in the Si cap due to stain relaxation. For plan view TEM, bevels have been previously formed on Si cap/700 nm Ge/Si bulk structures by conventional ion milling removing the underneath Si bulk and Ge layers in order to only characterize the defectivity in the Si cap.

## 3. Si cap layers characterization

### 3.1. Si–Ge intermixing

Si–Ge intermixing has been reported recently during Si cap growth on Ge using silane and trisilane based processes [9,21]. The presence of Ge in Si is explained by a Ge segregation mechanism enhanced by the difference between the Ge and Si surface energies, as already described in the case of Ge on Si or Si on Ge Molecular Beam Epitaxial or CVD growths [22–25].

Fig. 4 compares Ge profiles in 10MLs Si cap (after alignment of the profiles along the Si/Ge initial interface) grown with different processes using DCS at 650 °C, silane at 500 °C, and various

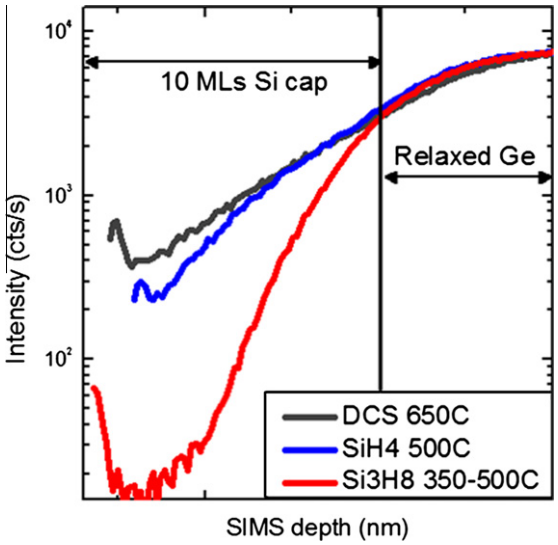


**Fig. 4.** Comparison of Ge segregation in Si by EXLE SIMS for Si cap grown with DCS at 650 °C, silane at 500 °C and trisilane at 350–500 °C. Ge segregation is severely reduced with trisilane precursor.

trisilane processes at 350–500 °C, respectively. The Ge slope in Si cap is independent on temperatures in the 350–500 °C range when trisilane is used as Si precursor [21]. A slightly higher Ge segregation is observed when Si cap is grown at 650 °C with DCS, as compared to the growth done at 500 °C with silane. The difference in temperature is considered as the main cause explaining the slightly different Ge slopes. However, the steepness of the Ge slope is severely reduced when trisilane is used at lower temperatures than 500 °C. The specific growth mechanism of trisilane on the H passivated surface explains a difference in Ge segregation probability. The H environment indeed impacts on the surface segregation as detailed in [24]. The interaction of the passivating H atoms and the trisilane molecules (which permits growth at low temperature for high order silanes precursor [26]) induces a lower Ge segregation rate. We note that the Ge slope obtained in the trisilane case was 0.8 nm/dec, which represents now the lowest steepness obtained by our SIMS measurements. As we approach here the limits of the SIMS technique, the Si–Ge intermixing might even be less than indicated based on the SIMS profile, i.e. a steeper or even more abrupt profile might be present for this process.

### 3.2. Defectivity

#### 3.2.1. Point defects formation

Very low temperature Si growth is generally expected to introduce point defects in the grown layers, cfr the observation of vacancy clusters for MBE [27].

Low temperatures (350–500 °C) Si homoepitaxy using trisilane has been recently reported as process with high defectivity [14]. Specific structures have been defined for Photoluminescence (PL) measurements using the following stack: Si cap/SiGe/Si seed layer/Si substrates. The process conditions of the Si seed layer have been varied to study its impact on PL sensitivity. Hole–electron pair radiative recombination only occurred when the growth temperature of the Si seed layer, grown with silane or DCS, was higher than 500 °C; all the seed layers grown at lower temperatures with trisilane provided non-radiative recombination and no PL emission in SiGe. This previous measurements indicate that Si layers grown with $Si_3H_8$ at 500 °C or lower temperatures are defective.

In the case of ultrathin Si caps grown on Ge, we compared the quality of Si layers grown at 350 and 450 °C using trisilane by the use of Second Harmonic Generation. Fig. 5 compares the SHG responses for different Si cap thicknesses grown at both temperatures. We note a very poor response for the Si caps grown at 350 °C, far from the perfect sinusoidal signal expected in case of centrosymmetric materials characterization. Increasing the growth temperature to 450 °C gives however a response in perfect agreement with SHG models as detailed in [20], whatever the Si thickness. The perfect sinusoidal response from the latter samples definitely highlights a better epitaxial growth quality as compared to the Si grown at 350 °C. The fact that the difference in response signal for the layers grown at 350 and 450 °C is also observed for very thin Si caps (thinner than the expected critical thickness for plastic relaxation), is attributed to point defects in the layers (such as vacancy clusters) and not to relaxation defects such as misfit or threading dislocations.

#### 3.2.2. Strain relaxation

The critical thickness for plastic relaxation for tensely strained Si layers grown on Ge has been discussed by several authors [7,8,28]. It has been recently determined by Raman spectroscopy around 0.8 nm (6MLs) when relaxation occurs via 90° partial dislocations generation and 1.4 nm (11.7MLs) when relaxation occurs via 60° perfect dislocations [7].

For various growth processes (here shown for growth temperatures of 450 °C and 500 °C), Fig. 6 illustrates the SHG response

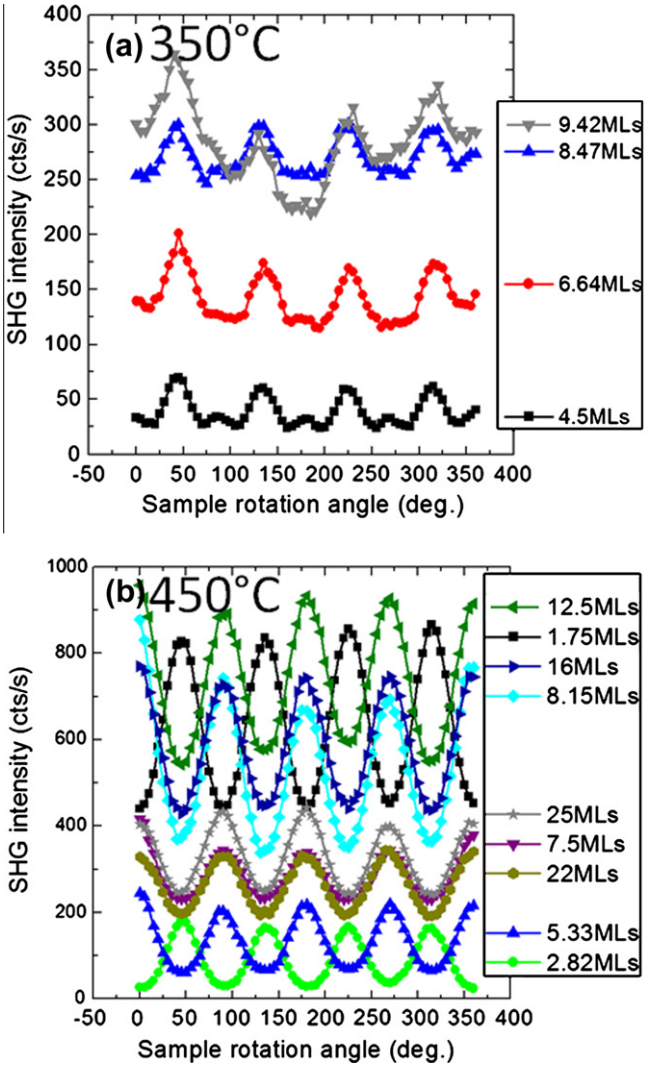


**Fig. 5.** SHG response of Si cap/Ge for different Si thicknesses and grown with trisilane at 350 and 450 °C. Better SHG response at 450 °C reveals a better Si epitaxial quality as compared to caps grown at 350 °C.

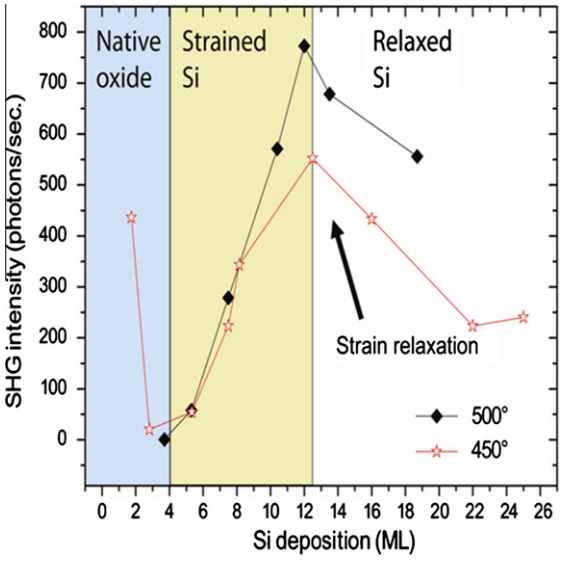


**Fig. 6.** SHG intensity response as a function of Si monolayers deposited for different Si cap growth processes. Maximal Si peak intensity at 12MLs identifies the critical thickness of plastic relaxation.

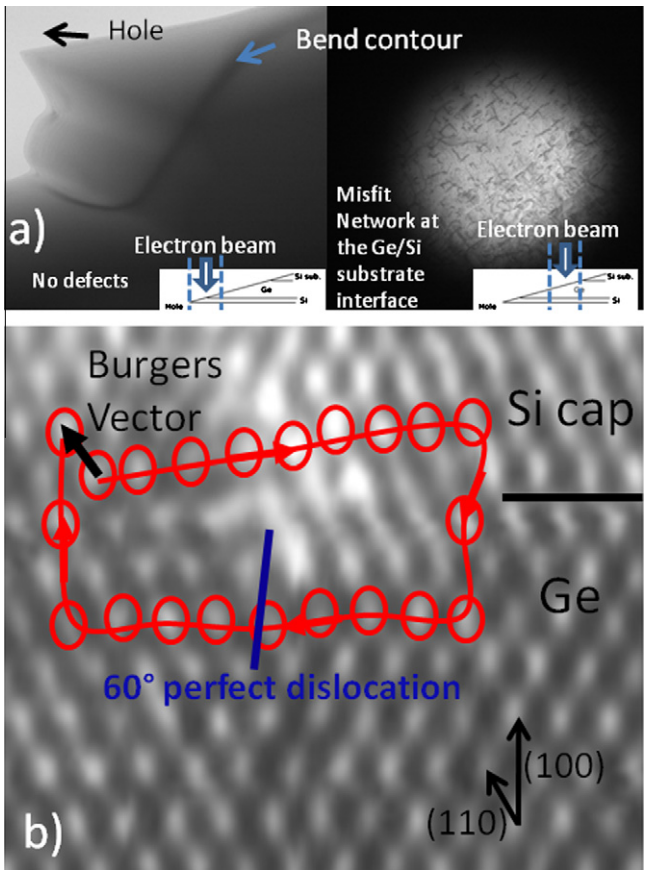


**Fig. 7.** (a) Plan view TEM analysis of a 11ML Si cap grown on Ge: no relaxation defects are identified in Si cap. (b) Cross section TEM on thick Si cap grown on Ge: identification of 60° perfect relaxation dislocation at the Si/Ge interface.

intensity as a function of the Si cap thickness. A maximal intensity is observed at 12MLs whatever the Si growth process used. We attribute this change of crystal symmetry occurring at 12MLs, as revealed by SHG, to plastic relaxation and associated defects formation as misfit dislocation. The critical thickness for plastic relaxation is then determined to be 12MLs.

Plan view TEM performed on a 11MLs Sicap/Ge sample with Si cap grown at 500 °C with trisilane indeed did not reveal any relaxation defects in the Si cap, as shown in Fig. 7a). Note that in the part of the layer where the Ge was not completely removed by ion milling, a misfit dislocation network could be identified in the Ge layer.

Thicker Si cap layers grown on Ge have been inspected by cross section TEM. In that case, relaxation defects have been observed at the Sicap/Ge interface. In Fig 7b), the dislocation burgers vector has been determined by drawing a clockwise Burgers circuit, as explained in [29]. The Burgers vector direction along the (1 1 0) indicates that the tensile strain in Si cap is released via 60° perfect dislocation formation. No stacking faults-90° partial dislocation have been observed, as normally formed during relaxation of compressively strained layers [30].

## 4. Discussion and conclusion

Many characteristics of the Si cap layers grown on Ge substrates have been identified and are proposed to explain the dependency of Ge pMOSFET electrical performances on Si cap growth processes.

The critical thickness for plastic relaxation of the Si cap grown on Ge has been determined to be 12MLs. Thinner Si caps are considered to be free of relaxation defects such as dislocations. For thicker layers, strain relaxation has been identified by the creation of a 60° perfect dislocation.

The difference in epitaxial quality has however been highlighted for similar Si cap thicknesses, grown with different processes. Especially, the very low temperature growth at 350 °C with trisilane leads to the presence of point defects in the Si layers. The presence of these defects in the Si cap is likely the cause of the lower hole mobility values observed in Ge pMOSFETs passivated with this Si cap process as compared to the passivated ones at higher temperature (500 °C) with silane [11]. Increasing the growth temperature and keeping trisilane as Si precursor however permits to improve the epitaxial quality, as shown by SHG characterization.

Differences in CET and $D_{IT}$ values in Ge pMOSFETs using either silane or trisilane processes are more likely linked to the amount of Ge present in Si cap as induced by a Ge surface segregation mechanism. If the Ge segregation rate is almost similar in Si cap grown with silane at 500 °C and DCS at 650 °C, trisilane at lower temperatures than 500 °C permits to reduce severely the amount of Ge in Si cap.

For Ge passivation purposes, this paper identifies the benefits and drawbacks of different Si cap processes using different Si precursors. From a scalability point of view, we have highlighted the interests in low temperatures ($\leqslant$500 °C) trisilane processes reducing the amount of Ge in Si caps. From a performance (mobility) point of view, higher temperature processes ($\geqslant$450–500 °C) are required to provide a much better Si cap epitaxial quality.

## Acknowledgements

The authors would like to acknowledge Voltaix for providing Trisilane to imec. We acknowledge the European Commission for financial support in the DualLogic Project No. 214579. Further, we thank the imec core partners within the imec's Industrial Affiliation Program on Logic. For Second Harmonic Generation measurement done at K.U. Leuven, we acknowledge financial support from the Fund for scientific research Flanders (FWO-V), the University of Leuven (GOA), Methusalem Funding by the Flemish government and the Belgian Inter-University Attraction Poles IAP Programmes. V.K. Valev is grateful for the support from the FWO-Vlaanderen.

## References

[1] Heyns M, Tsai W. MRS Bull 2009;34(7):485–92.
[2] Caymax M, Eneman G, Bellenger F, Merckling C, Delabie A, Wang G, et al. In: Tech dig-int election devices meet 2009.
[3] Bellenger F, De Jaeger B, Merckling C, Houssa M, Penaud J, Nyns L, et al. Electron Dev Lett 2010;31(5):402–4.
[4] Martinez E, Renault O, Clavelier L, Le Royer C, Hartmann J-M, Loup V, et al. J Vac Sci Technol B 2007;25(1):86–90.
[5] Houssa M, Nelis D, Hellin D, Pourtois G, Conard T, Paredis K, et al. Appl Phys Lett 2007;90:222105.
[6] Kamata Y, Takashima A, Kamimuta Y, Tezuka T. VLSI Dig Tech Pap 2009:78.
[7] Fang Y-Y, D'Costa VR, Tolle J, Poweleit CD, Kouvetakis J, Menendez J. Thin Solid Films 2008;516:8327.
[8] Hartmann JM, Abbadie A, Cherkashin N, Grampeix H, Clavelier L. Semicond Sci Technol 2009;24:055002.
[9] Caymax M, Leys F, Mitard J, Martens K, Yang L, Pourtois G, et al. J Electrochem Soc 2009;156:H979.
[10] Mitard J, Vincent B, De Jaeger B, Krom R, Loo R, Eneman G, et al. ECS Trans 2010;28(2):157–69.
[11] Mitard J, Shea C, De Jaeger B, Pristera A, Wang G, Houssa M, et al. VLSI Dig Tech Pap 2009.
[12] Mitard J, De Jaeger B, Leys FE, Hellings G, Martens K, Eneman G, et al. In: Tech dig-int election devices meet 2008.
[13] Brunco DP, De Jaeger B, Eneman G, Mitard J, Hellings G, Satta A, et al. J Electrochem Soc 2008;155:H552.
[14] Vincent B, Loo R, Vandervorst W, Brammertz G, Caymax M. J Cryst Growth 2010;312:2671–6.
[15] Vandervorst W et al. Mater Res Soc Symp Proc 2004;809.
[16] Wang W-E, Balooch M, Claypool C, Zawaideh M, Farnaam K. Solid State Technol 2009:18.

[17] Loo R, Wang G, Souriau L, Lin JC, Takeuchi S, Brammertz G, et al. J Electron Soc 2010;157(1):H13–21.
[18] Vandervorst W. Appl Surf Sci 2008;255:805.
[19] Valev VK, Leys FE, Caymax M, Verbiest T. Appl Phys Lett 2009;94:061123.
[20] Valev VK, Vanbel MK, Vincent B, Moshchalkov VV, Caymax M, Verbiest T. Electron Dev Lett 2011;32(1).
[21] Vincent B, Vandervorst W, Caymax M, Loo R. Appl Phys Lett 2009;95:262112.
[22] Tsu R, Xiao HZ, Kim YW, Hasan MA, Birnbaum HK, Greene JE, et al. J Appl Phys 1994;75(1):240–7.
[23] Nakagawa K, Miyao M. J Appl Phys 1991;69(5):3058–62.
[24] Rudkevich E, Liu F, Savage DE, Kuech TF, Mc Caughan L, Lagally MG. Phys Rev Lett 1998;81(16):3467–70.
[25] Lin DS, Miller T, Chiang TC. Phys Rev B 1992;45(19):415–8.
[26] Sturm JC, Chung KH. ECS Trans 2008;16(10):799–805.
[27] Asoka-Kumar P, Gossmann HJ, Unterwald FC, Feldman LC, Leung TC, Au HL, et al. Phys Rev B 1993;48(8).
[28] People R, Bean JC. Appl Phys Lett 1985;47:322.
[29] Sakai A, Tatsumi T, Aoyama K. Appl Phys Lett 1997;71:24.
[30] Vincent B, Damlencourt JF, Delaye V, Gassilloud R, Clavelier L, Morand Y. Appl Phys Lett 2007;90:074101.