CHAPTER
FOUR

OXIDATION

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4.1 INTRODUCTION

The oxidation of silicon is necessary during the entire process of fabricating modern integrated circuits. The production of high-quality ICs requires not only an understanding of the basic oxidation mechanism, but the ability to form, in a controlled and repeatable manner, a high-quality oxide. In addition, to ensure the reliability of the ICs, the electrical properties of the oxide must be understood.

Silicon dioxide has several uses: to serve as a mask against implant or diffusion of dopant into silicon, to provide surface passivation, to isolate one device from another (dielectric isolation as opposed to junction isolation), to act as a component in MOS structures, and to provide electrical isolation of multilevel metallization systems. Several techniques for forming the oxide layers have been developed such as thermal oxidation, wet anodization, vapor phase technique [chemical vapor deposition (CVD)], and plasma anodization or oxidation. When the interface between the oxide and the silicon is required to have a low charge density level, thermal oxidation has been the preferred technique. However, since the masking oxide is generally removed, this consideration is not as important in the case of masking against diffusion of dopant into silicon. Obviously when the oxide layer is required on top of a metal layer, as in the case of a multilevel metallization structure, the vapor phase technique is uniquely suited. This chapter concentrates on thermal silicon oxidation, because it is the principal technique used in IC processing.

In this chapter we describe the oxidation process to provide a foundation for understanding the kinetics of growth and interface properties. Section 4.2 examines the oxidation model and its fit to experimental data; the effect of orientation, dopant concentration, and HCl addition to the ambient; and surface damage on the kinetics of

oxidation. Section 4.3 describes standard thermal oxidation techniques, such as dry, wet, and HCl dry as well as the less familiar high-pressure and plasma oxidation techniques. It also describes the cleaning processes needed to remove surface contamination prior to oxidation. Section 4.4 covers the characteristics and properties of oxides, with emphasis on oxide masking, oxide charges, and stresses in thermal oxides. Sections 4.5 and 4.6 examine the redistribution of dopants at the Si-SiO_2 interface during thermal oxidation and during oxidation of polysilicon, respectively. Section 4.7 considers oxidation-induced stacking faults and oxide isolation defects. A summary and a discussion of the future trends are presented in the last section.

4.2 GROWTH MECHANISM AND KINETICS

Since a silicon surface has a high affinity for oxygen, an oxide layer rapidly forms when it is exposed to an oxidizing ambient. The chemical reactions describing the thermal oxidation of silicon[1] in oxygen or water vapor are given in Eqs. 1 and 2, respectively.

$$\mathrm{Si(solid)} + O_2 \rightarrow \mathrm{SiO_2(solid)} \quad (1)$$

$$\mathrm{Si(solid)} + 2H_2O \rightarrow \mathrm{SiO_2(solid)} + 2H_2 \quad (2)$$

The basic process involves shared valence electrons between silicon and oxygen; the silicon-oxygen bond structure is covalent. During the course of the oxidation process the Si-SiO_2 interface moves into the silicon; however, the volume expands, resulting in the external SiO_2 surface not being coplanar with the original silicon surface. Based on the densities and molecular weights of Si and SiO_2, we can show that for growth of an oxide of thickness d, a layer of silicon $0.44d$ thick is consumed (Fig. 1).

The framework of a model to describe silicon oxidation has been created. Radioactive tracer,[1] marker,[2] and infared isotope shift[3] experiments have established that oxidation proceeds by the diffusion of the oxidizing species through the oxide to the Si-SiO_2 interface, where the oxidation reaction occurs. Uncertainties exist, however, as evidenced by controversies in the literature as to whether charged or neutral species are transported through the oxide, and on the details of the reaction at the Si-SiO_2 interface.

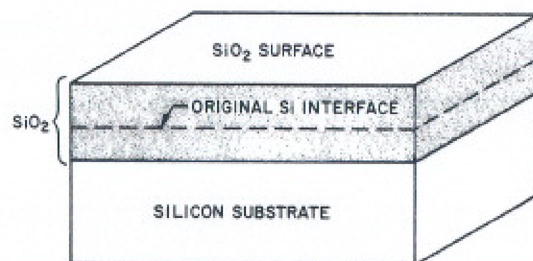

Fig. 1 Growth of SiO_2.

4.2.1 Silicon Oxidation Model

Deal and Grove's model describes the kinetics of silicon oxidation.[4] It is generally valid for temperatures between 700 and 1300°C, partial pressures between 0.2 and 1.0 atm (perhaps higher), and oxide thicknesses between 300 and 20,000 Å for oxygen and water ambients. Figure 2 shows the silicon substrate covered by an oxide layer that is in contact with the gas phase. The oxidizing species (1) are transported from the bulk of the gas phase to the gas-oxide interface with flux F_1 (the flux is the number of atoms or molecules crossing a unit area in a unit time), (2) are transported across the existing oxide toward the silicon with flux F_2, and (3) react at the Si-SiO_2 interface with the silicon with flux F_3.

For steady state, $F_1 = F_2 = F_3$. The gas-phase flux F_1 can be linearly approximated by assuming that the flux of oxidant from the bulk of the gas phase to the gas-oxide interface is proportional to the difference between the oxidant concentration in the bulk of the gas C_G and the oxidant concentration adjacent to the oxide surface C_S.

$$F_1 = h_G (C_G - C_S) \quad (3)$$

where h_G is the gas-phase mass-transfer coefficient.

To relate the equilibrium oxidizing species concentration in the oxide to that in the gas phase, we invoke Henry's law,

$$C_0 = Hp_s \quad (4)$$

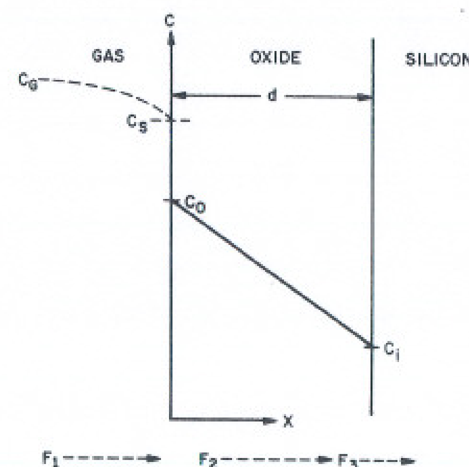

Fig. 2 Basic model for thermal oxidation of silicon. *(After Deal and Grove, Ref. 4.)*

and

$$C^* = Hp_G \tag{5}$$

where C_0 is the equilibrium concentration in the oxide at the outer surface, C^* is the equilibrium bulk concentration in the oxide, p_s is the partial pressure in the gas adjacent to the oxide surface, p_G is the partial pressure in the bulk of the gas, and H is Henry's law constant. Using Henry's law along with the ideal gas law[5] allows us to rewrite C_G and C_C

$$C_G = \frac{p_G}{kT} \tag{6a}$$

$$C_S = \frac{p_s}{kT} \tag{6b}$$

Combining Eqs. 3 to 6 gives

$$F_1 = h(C^* - C_0) \tag{7}$$

where h is the gas-phase mass-transfer coefficient in terms of concentration in the solid, given by $h = h_G/HkT$. When the concentration of the oxidant in the oxide at the oxide-gas interface C_0 is less than the equilibrium bulk oxide concentration, F_1 is positive. Oxidation is a nonequilibrium process with the driving force being the deviation of concentration from equilibrium.[6] Henry's law is valid only in the absence of dissociation effects at the gas-oxide interface. This implication is that the species moving through the oxide is molecular.

The flux of this oxidizing species across the oxide is taken to follow Fick's law

$$F_2 = -D\frac{dC}{dd} \tag{8}$$

at any point d in the oxide layer. D is the diffusion coefficient and dC/dd is the concentration gradient of the oxidizing species in the oxide. Following the steady-state assumption, F_2 must be the same at any point within the oxide (i.e., $dF_2/dd = 0$) resulting in

$$F_2 = \frac{D(C_0 - C_i)}{d_0} \tag{9}$$

where C_i is the oxidizing species concentration in the oxide adjacent to the oxide-silicon interface and d_0 is the oxide thickness.

Assuming that the flux corresponding to the Si-SiO_2 interface reaction is proportional to C_i

$$F_3 = k_s C_i \tag{10}$$

where k_s is the rate constant of chemical surface reaction for silicon oxidation.

After setting $F_1 = F_2 = F_3$, as dictated by steady-state conditions, and solving simultaneous equations, we obtain the following expressions for C_i and C_0:

$$C_i = \frac{C^*}{1 + \dfrac{k_s}{h} + \dfrac{k_s d_0}{D}} \tag{11}$$

$$C_0 = \frac{\left[1 + \dfrac{k_s d_0}{D}\right]C^*}{1 + \dfrac{k_s}{h} + \dfrac{k_s d_0}{D}} \tag{12}$$

The limiting cases of Eqs. 11 and 12 arise when the diffusivity is either very small or very large. When the diffusivity is very small, $C_i \to 0$ and $C_0 \to C^*$. This case is called the diffusion-controlled case. It results from the flux of oxidant through the oxide being small (due to D being small) compared to the flux corresponding to the Si-SiO_2 interface reaction. Hence the oxidation rate depends on the supply of oxidant to the interface, as opposed to the reaction at the interface.

In the second limiting case, where D is large, $C_i = C_0 = C^*/(1+k_s/h)$. This is called the reaction-controlled case, because an abundant supply of oxidant is provided at the Si-SiO_2 interface, and the oxidation rate is controlled by the reaction rate constant k_s and by C_i (which equals C_0).

To calculate the rate of oxide growth, we define N_1 as the number of oxidant molecules incorporated into a unit volume of the oxide layer. Since the oxide has 2.2×10^{22} SiO_2 molecules/cm^3 and one O_2 molecule is incorporated into each SiO_2 molecule, whereas two H_2O molecules are incorporated into each SiO_2 molecule, N_1 equals 2.2×10^{22} cm^{-3} for dry oxygen and twice this number for water-vapor oxidation. Combining Eqs. 10 and 11 along with the definition of flux, the flux of oxidant reaching the oxide-silicon interface is given by

$$N_1 \frac{dd_0}{dt} = F_3 = \frac{k_s C^*}{1 + \dfrac{k_s}{h} + \dfrac{k_s d_0}{D}} \tag{13}$$

We solve this differential equation assuming that an oxide may initially be present from a previous processing step or it may grow before the assumptions in the model are valid, that is, $d_0 = d_i$ at $t = 0$. The solution of Eq. 13 is

$$d_0^2 + Ad_0 = B(t + \tau) \tag{14}$$

where

$$A = 2D\left[\frac{1}{k_s} + \frac{1}{h}\right] \tag{14a}$$

$$B = \frac{2DC^*}{N_1} \tag{14b}$$

$$\tau = \frac{d_i^2 + Ad_i}{B} \tag{14c}$$

The quantity τ represents a shift in the time coordinate to account for the presence of the initial oxide layer d_i. Equation 14 is the well-known, mixed linear-parabolic relationship.[7]

Solving Eq. 14 for d_0 as a function of time gives

$$\frac{d_0}{A/2} = \left[1 + \frac{t + \tau}{A^2/4B}\right]^{1/2} - 1 \tag{15}$$

One limiting case occurs for long oxidation times when $t >> \tau$.

$$d_0^2 = Bt \tag{16}$$

Equation 16 is the parabolic law, where B is the parabolic rate constant. The other limiting case occurs for short oxidation times when $(t + \tau) << A^2/4B$.

$$d_0 = \frac{B}{A}(t + \tau) \tag{17}$$

Equation 17 is the linear law, where B/A is the linear rate constant given by

$$\frac{B}{A} = \left[\frac{k_s h}{k_s + h}\right]\left[\frac{C^*}{N_1}\right] \tag{18}$$

Equations 16 and 17 are the diffusion-controlled and reaction-controlled cases, respectively.

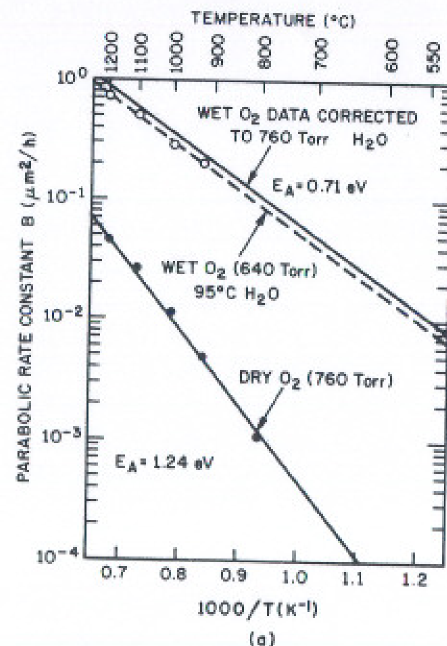

Fig. 3(a) The effect of temperature on the parabolic rate constant for dry and wet oxygen.

4.2.2 Experimental Fit

This section compares Deal and Grove's model to their experimental measurements. Deal and Grove used (111) oriented, lightly boron-doped silicon wafers, that were cleaned prior to oxidation in purified dry oxygen (less than 5-ppm water content) or in wet oxygen (the partial pressure of water was 640 Torr). For wet oxygen oxidation they found that $d_i = 0$ at $t = 0$ by plotting oxide thickness versus oxidation time. Algebraically manipulating Eq. 14 and using the plot of wet oxygen data, they graphically obtained the rate constants. Table 1 lists the values of these rate constants for wet oxidation of silicon.[4] The absolute value of A increases with decreasing temperature, while the parabolic rate constant B decreases with decreasing temperature (Figs. 3a and b).

For dry O_2 a plot of oxide thickness versus oxidation time does not extrapolate to zero initial thickness, but instead to a value which equals about 250 Å for data spanning a range of 700 to 1200°C. The faster initial oxidation rate during the initial phase of oxidation implies a different mechanism in this region. Thus use of Eq. 14 for dry oxidation requires a value for τ that can be generated graphically by extrapolating the linear region back to the time axis. Problems arise at higher temperatures where the linear-parabolic or parabolic ranges are encountered, in which case the

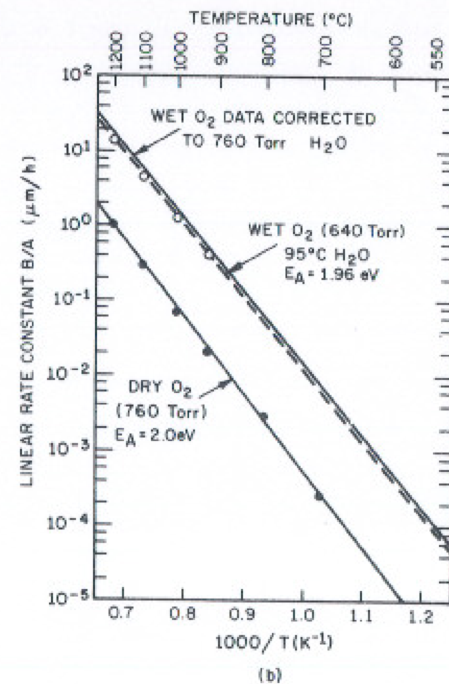

Fig. 3((b) The effect of temperature on the linear rate constant. *(After Deal and Grove, Ref. 4.)*

Table 1 Rate constants for wet oxidation of silicon

Oxidation temperature (°C)	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B/A (μm/h)	τ (h)
1200	0.05	0.720	14.40	0
1100	0.11	0.510	4.64	0
1000	0.226	0.287	1.27	0
920	0.50	0.203	0.406	0

value of τ as defined in Eq. 14 must be used. Table 2 lists the values of rate constants for dry oxidation of silicon.[4]

Examination of Eq. 14b reveals that B is expected to be proportional to C^*, which, according to Henry's law, is proportional to the partial pressure of the oxidizing species. However, A should be independent of the partial pressure. This has indeed been confirmed experimentally for both wet and dry oxidations[4,8] in the temperature range between 1000 and 1200°C and between 0.1 and 1 atm. The pressure independence of A means that the linear rate constant B/A has the same linear pressure dependence as B.

Figure 3a shows the effect of temperature[4] on the parabolic rate constant B for both dry and wet oxygen at 640 Torr and for wet oxygen normalized to 760 Torr using the linear pressure dependence. As might be expected from Eq. 14, the temperature dependence of B is similar to that of D, that is, B increases exponentially with temperature. For dry oxygen the activation energy for B is 1.24 eV, which is comparable to the value of 1.17 eV for the diffusivity of oxygen through fused silica (similar in structure to thermal SiO_2). The wet oxygen activation energy (0.71 eV) also compares favorably with the activation energy for the diffusivity of water in fused silicon (0.80 eV).

Figure 3b shows the temperature dependence of the linear rate constant B/A for both dry and wet oxygen at 640 Torr and for wet oxygen normalized to 760 Torr. Once again an exponential dependence is observed with activation energies 1.96 and 2.0 eV for wet and dry oxidation, respectively. Deal and Grove[4] show that these

Table 2 Rate constants for dry oxidation of silicon

Oxidation temperature (°C)	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B / A (μ/h)	τ (h)
1200	0.040	0.045	1.12	0.027
1100	0.090	0.027	0.30	0.076
1000	0.165	0.0117	0.071	0.37
920	0.235	0.0049	0.0208	1.40
800	0.370	0.0011	0.0030	9.0
700	...	...	0.00026	81.0

Table 3 C^* values in SiO_2 at 1000°C

Species	C^* (cm^{-3})
O_2	5.2×10^{16}
H_2O	3.0×10^{19}

values reflect the temperature dependence of the interface reaction-rate constant k_s. As stated previously, in the linear range the reaction is reaction controlled. Similar values were obtained for the linear rate constants for both dry and wet oxidations, indicating a similar reaction or surface control mechanism. Interestingly, the above values are comparable to the 1.83 eV required to break a Si—Si bond.

The equilibrium concentration C^* of the oxidizing species in SiO_2 can be calculated from Eq. 14b by using appropriate values for B, D, and N_1. Table 3 gives an example.[4]

Even though the diffusivity of water in SiO_2 is lower than that of oxygen,[4] the parabolic rate constant B is substantially larger for wet oxidation than for dry. This is the major reason why the parabolic oxidation rate in steam is faster than in dry oxygen; the flux of oxidant, and hence B, is proportional to C^*, which is approximately three orders of magnitude greater for water than for oxygen (see Table 3). Furthermore, since the linear rate constant B/A also is related to B and hence C^*, we can also attribute the faster linear oxidation rate for wet oxidation to the above mechanism.

Deal and Grove's simple model (Eqs. 14 and 15) for thermal silicon oxidation provides excellent agreement with various normalized experimental data[4] for both wet and dry oxidations. The only exception is for SiO_2 films less than about 300 Å thick grown in dry oxygen. In this case an anomalously high oxidation rate is observed with respect to the model.

4.2.3 Diffusing Species and Interface Considerations

The excellent agreement between the model and experimental observations supports the use of Henry's law. This implies the lack of dissociative effects at the gas-SiO_2 interface indicating the species diffusing in the oxide is molecular for both oxygen (dry) and steam (water-vapor) oxidations. Additional results[9] indicate that the oxidant is molecular for both water and oxygen oxidations, since good agreement is obtained between the calculated (for fused silica) and measured oxidation rates (for oxidation of silicon) with respect to absolute rate and pressure, and with respect to temperature dependence.

A proposed modification[10] to the Deal-Grove model provides an excellent fit to the experimental data, including the thin, dry oxidation regime where the Deal-Grove model breaks down. The physical basis of the proposed model is that while diffusion through the oxide is still by molecular oxygen, the oxidation of silicon occurs by the reaction of a small concentration of atomic oxygen.

As stated earlier, the question of whether the oxidizing species is charged or neutral is still a subject of controversy. While the above discussion favors diffusion of a

molecular species, supportive evidence[2] for a charged species arises from experiments showing that an applied electric field can influence the oxidation rate, either accelerating it or retarding it, depending on whether the silicon is positive or negative with respect to the oxide-gas interface. Another work,[11] based on studies of electrical conduction at elevated temperatures, concludes that the species responsible for ionic conduction is doubly negative interstitial oxygen ions (O_i^{2-}).

We now shift our discussion from the unresolved question of the nature of the diffusant to the Si-SiO_2 interface. The structure and oxidation mechanism at the interface is particularly important since what occurs here from an atomistic point of view can influence not only the oxidation kinetics but also allied areas of interest, such as diffusion. Both the interface structure and its oxidation mechanisms are complicated and a continuing source of discussion in the literature.

The controversies as to whether charged or neutral species are transported through the oxide have been reviewed[12, 14] followed by the proposal of a model that appears consistent with much of the earlier data. The model is based on a large molecular volume difference between Si and SiO_2. This difference must be accommodated to allow a newly formed SiO_2 molecule to fit into the normal SiO_2 structure. This leads to the proposal of an interface transition region, which consists of a network of extra half planes that terminate at the Si side of the Si-SiO_2 interface. Movement of this interface requires a supply of vacancies from the silicon to the interface, the movement of Si interstitials from the interface into the bulk Si, or free volume influx from the SiO_2 (i.e., viscous flow).[12–14] An additional proposal[14] relating to the interface suggests that silicon is transformed to α-cristobalite plus interstitial Si ions. Subsequent oxidation of the interstitials produces lattice distortion and transformation to vitrous silica. Hence the crystalline SiO_2 phase exists only as a buffer between the Si and vitrous SiO_2. The proposed interface mechanisms are consistent with qualitative explanations related to oxidation-enhanced diffusion, stacking fault formation, interface charge, and oxidation velocity.

Additional mechanisms have been proposed, which attempt to explain point-defect-related interface phenomena. The presence of doubly negative interstitial oxygen ions (O_i^{2-}) was discussed previously. Such ions at the Si-SiO_2 interface may react with silicon and displace it to an interstitial position in the lattice to form Si_I—O, which can combine to form SiO_2. A silicon interstitial flux can occur if the Si_I—O pair dissociates before forming SiO_2.[15] Such an incomplete oxidation occurs for one out of every thousand silicon atoms.[16] Although the interface reaction generally goes to completion, even a small flux of silicon interstitials into the silicon can have a large effect on defect formation or diffusion. The case of O_i^{2-} reacting with vacancies, as supplied from the silicon substrate, could lead to a vacancy flux. Such a process may be significant in the case of heavy doping.

4.2.4 Thin Oxide Growth

As noted earlier, the structure of the oxide very close to the silicon-oxide interface and the oxidation process itself both involve uncertainties. Our understanding is further complicated by the observation of an initial rapid oxidation for the case of dry

oxide growth, which causes the linear portion of the oxide growth versus time curve to extrapolate to an initial thickness of about 200 Å.

With advanced MOS structures the ability to grow, with reproducible results, thin ⩽300-Å, uniform, high-quality gate oxides has become increasingly important. In another application, thin pad oxides of thicknesses between 50 and 1000 Å have been used routinely under masking nitride layers to prevent stress-induced defects in the underlying silicon. The discussion in this section concentrates on the techniques and properties of thin oxides.

The technology for thin oxide growth is still emerging with a variety of techniques being used. Aside from the kinetics of oxide growth, other properties studied typically include refractive index, oxide composition, etch rate, density, susceptibility to pinholes, stress, and dielectric breakdown.

From a practical point of view, thin oxide growth must be slow enough to obtain uniformity and reproducibility. Various growth techniques include dry oxidation, dry oxidation with HCl, sequential oxidations using different temperatures and ambients, wet oxidation, reduced pressure techniques, and even high-pressure, low-temperature oxidations. The oxidation rate will, of course, be lower at lower temperatures and reduced pressures. Ultrathin oxides (<50 Å) have been produced using hot nitric acid, boiling water, and air at room temperature. For whatever technique is chosen, the desired properties must be obtained.

In discussing the techniques used and properties obtained it should be emphasized that thin oxide growth is influenced by the cleaning techniques used[17] and the purity of the gases used (especially moisture content). Figure 4 shows an example of thin oxide growth versus oxidation time in dry oxygen.[18] This data demonstrates that a set

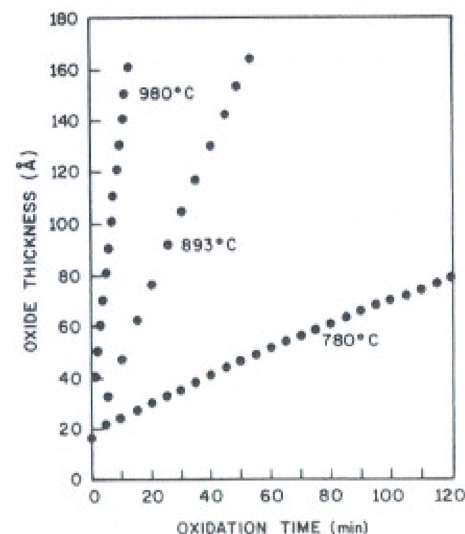

Fig. 4 Oxide thickness versus oxidation time at 780, 893, and 980°C in dry oxygen. *(After Irene, Ref. 18.)*

of time-temperature conditions can be chosen to grow thin oxides compatible with reasonable throughput.

Processing conditions have an important impact on oxide properties. For example, oxide density increases as the oxidation temperature is reduced.[19] Additionally, HCl ambients have typically been used to passivate ionic sodium, improve the breakdown voltage, and getter impurities and defects in the silicon. This passivation effect only begins to occur in the higher temperature range. A two-step process sequence has been devised[20] in which a uniform, reproducible oxide of small defect density is formed at a moderate temperature (1000°C or less) using a dry O_2, HCl ambient. The second step consists of a heat treatment in N_2, O_2, and HCl at 1150°C to provide passivation and to bring the oxide thickness to the desired level. Such a processing scheme takes advantage of beneficial effects occurring in both the lower and higher temperature ranges.

Reduced pressure oxidation offers an attractive way of growing thin oxides in a controlled manner. Oxides between 30 and 140 Å thick have been grown in a CVD reactor at 900 to 1000°C using oxygen at a pressure of 0.25 to 2.0 Torr.[21] The observed kinetics are parabolic, and the rate constants agree with values extrapolated from atmospheric pressure. Oxides obtained by this technique etch at the same rate as dry oxides obtained at 950°C and 1 atm. The equal etch rate indicates a similar oxide composition and structure between the two oxides. The intrinsic breakdown fields are high (10 to 13 MV/cm) and distributed over a narrow range. All indications are that the reduced pressure oxides are very uniform, homogeneous, and similar to thicker oxides prepared at atmospheric pressure.

As a final example of thin oxide growth, we consider the use of high-pressure, low-temperature steam oxidation of silicon. At 10-atm pressure and 750°C, a 300-Å-thick oxide can be grown in 30 min. Obviously the time, temperature, and pressure can be changed to vary the thickness. Such a technique has been applied to the growth of a thin gate oxide in the process to fabricate MOS dynamic RAMs.[22] At the same time the thin oxide layer was grown, a thick oxide layer was grown over a doped polysilicon layer as a result of concentration-enhanced oxidation. The properties of the oxides depended on the oxidation temperature rather than pressure. For example, oxide density and refractive index decreased whereas chemcial etch rate and residual stress increased with increasing temperature. The temperature and pressure ranges were 700 to 1000°C and approximately 5 to 10 atm, respectively.

4.2.5 Orientation Dependence of Oxidation Rates

Experiments have indicated that the oxidation kinetics are a function of the crystallographic orientation of the silicon surface.[23] This relationship is attributed to the orientation dependence of k_s (Eqs. 10 and 14a) and manifests itself in an orientation-dependent linear rate constant. The linear rate constant is related to the interface reaction kinetics and depends on the rate at which silicon atoms are incorporated into the oxide. This depends on the silicon surface atom concentration, which is orientation dependent. As might be expected, the parabolic rate constant B is independent of silicon surface orientation,[24] since B is diffusion limited. Figure 5 shows[25] oxide

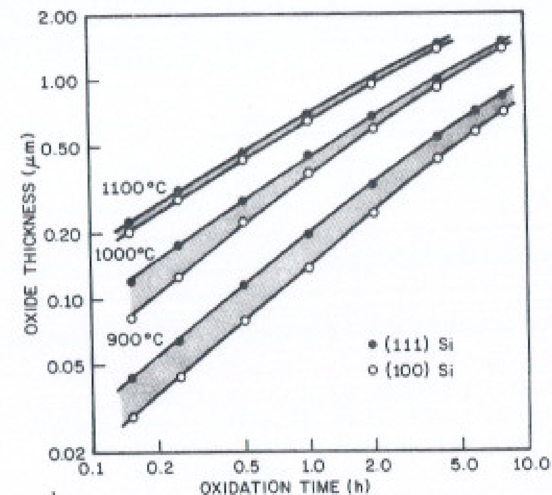

Fig. 5 Oxide thickness versus oxidation time for silicon in H_2O at 640 Torr. *(After Deal, Ref. 25.)*

thickness as a function of oxidation time in water at 640 Torr for both (111) and (100) oriented silicon. Table 4 gives rate constants obtained from this data.[25] This data along with that for oxygen yields linear rate constants for (111) silicon that are 1.68 times those for (100) silicon at corresponding temperatures.

A model has been presented[23] to explain how the linear oxidation rate of the silicon depends on the orientation of the silicon surface. According to this model, a direct reaction occurs between a water molecule in the silica and a silicon-silicon bond at the Si-SiO_2 interface. At this interface all the silicon atoms are partially

Table 4 Rate constants for silicon oxidation in H_2O (640 Torr)

Oxidation temperature (°C)	Orientation	A (μm)	Parabolic rate constant B (μm²/h)	Linear rate constant B/A (μm/h)	B/A ratio (111)/(100)
900	(100)	0.95	0.143	0.150	
	(111)	0.60	0.151	0.252	1.68
950	(100)	0.74	0.231	0.311	
	(111)	0.44	0.231	0.524	1.68
1000	(100)	0.48	0.314	0.664	
	(111)	0.27	0.314	1.163	1.75
1050	(100)	0.295	0.413	1.400	
	(111)	0.18	0.415	2.307	1.65
1100	(100)	0.175	0.521	2.977	
	(111)	0.105	0.517	4.926	1.65
					Average 1.68

Table 5 Calculated properties of silicon crystal planes

Orientation	Area of unit cell (cm^2)	Si atoms in area	Si bonds in area	Bonds available	Bonds $\times 10^{14}$ cm^{-2}	Available bonds, N ($\times 10^{14}$ cm^{-2})	N rel[illegible] to (1[illegible]
(110)	$\sqrt{2}\,a^2$	4	8	4	19.18	9.59	1.00[illegible]
(311)	$1/8\sqrt{11}\,a^2$	1.5	3	2	24.54	16.36	1.70[illegible]
(111)	$1/2\sqrt{3}\,a^2$	2	4	3	15.68	11.76	1.22[illegible]
(100)	a^2	2	4	2	13.55	6.77	0.70[illegible]

bonded to silicon atoms below and to oxygen atoms above. The orientation dependence of the oxidation rate comes from terms representing the activation energy for oxidation and the concentration of reaction sites. This concentration depends on the concentration of silicon-silicon bonds *available* for reaction at a given time. The bond is directional so its availability depends on its angle relative to the surface plane, its position with respect to adjacent atoms, and the water molecule size being such that when reacting with some angled silicon-silicon bonds, it can screen adjacent bonds from other water molecules.[6] These and other geometric effects are called steric hindrances and result in the linear oxidation rate being orientation dependent. Table 5 lists calculated properties of four silicon planes.[23] The orientation dependence is related to the available bond density N and the orientation dependence of the activation energy.

As might be expected, steric hindrance results in higher activation energy. Experimental data has been analyzed to determine the apparent activation energy, which is the sum of two components: a term related to the enthalpy of solution of water in the silica films and the orientation-dependent term related to the activation energy of oxidation. Table 6 lists the values of some apparent activation energies.[23] The interaction between the available bond density and the activation energy determines the orientation dependence of the linear oxidation rates. Experiments[23] show that the oxidation rate v in steam is ordered in the following manner

$$v_{110} > v_{311} > v_{111}$$

with a slower rate predicted for the (100) orientation. Additional measurements[24] in steam show the following oxidation rate sequence

$$v_{111} > v_{110} > v_{311} > v_{100}$$

However, this set of measurements was made at a higher temperature than the former set.[22]

For dry oxidation a similar argument for steric hindrance can be made. The following sequence is experimentally obtained[26]

$$v_{110} \geqslant v_{111} > v_{100}$$

for the linear oxidation rate.

Table 6 Apparent activation energies

Orientation	Activation energy (eV)
(110)	1.23 ± 0.02
(311)	1.30 ± 0.03
(111)	1.29 ± 0.03

4.2.6 Effect of Impurities and Damage on the Oxidation Rate

Because wet oxidation occurs at a substantially greater rate than for dry oxidation, any unintentional moisture accelerates the dry oxidation. In fact, both the linear and parabolic oxidation rates are sensitive to the presence of water and other impurities. The effects of some of these impurities are discussed in the following sections.

Water Experiments were done to study the effect of intentionally adding 15-ppm water vapor to a process that normally used less than 1-ppm water.[25] A significant acceleration in the oxidation rate was observed. For example, an 800°C oxidation of (100) silicon for 700 minutes grew an oxide approximately 300 Å thick with less than 1-ppm moisture and an oxide approximately 370 Å thick with 25-ppm moisture. In these experiments the oxygen was from a liquid source and the oxidation chamber was a double-wall, fused-silica tube with N_2 flowing between the walls. A precombustor and cold trap were used to achieve the less than 1-ppm moisture level.

Sodium High concentrations of sodium influence the oxidation rate by changing the bond structure in the oxide, thereby enhancing the diffusion and concentration of the oxygen molecules in the oxide.[6]

Group III and V elements The common dopant elements in this group, when present in silicon at high concentration levels, can enhance the oxidation behavior. The dopant impurities are redistributed at the growing Si-SiO_2 interface.[27] This effect is discussed in greater detail in Section 4.5, but we consider it from a mechanism standpoint here. The effect results in a discontinuous concentration profile at the interface, that is, the dopant either segregates into the silicon or into the oxide. The redistribution of the impurity at the interface influences the oxidation behavior. If the dopant segregates into the oxide and remains there (which is the case for boron in an oxidizing ambient), the bond structure in the silica weakens. This weakened structure permits an increased incorporation and diffusivity of the oxidizing species through the oxide, thus enhancing the oxidation rate. Impurities that segregate into the oxide but then diffuse rapidly through it (such as aluminum, gallium, and indium) exhibit the same oxidation kinetics as lightly doped silicon. Figure 6 shows oxidation rate curves for various concentrations of boron for wet oxygen.[28] From the above discussion it is not surprising that an enhancement in the oxidation kinetics is observed where diffusion control predominates. For oxidation of phosphorous-doped silicon in wet oxygen,[28] a concentration dependence is observed only at the lower temperatures where

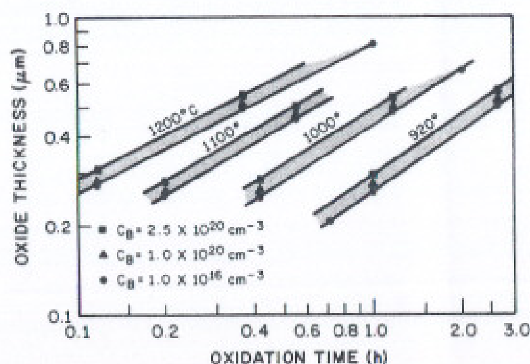

Fig. 6 Oxidation of boron-doped silicon in wet oxygen (95°C H_2O) as a function of temperature and concentration. *(After Deal and Sklar, Ref. 28.)*

the surface reaction becomes important (Fig. 7). This dependence may be the result of phosphorus being segregated into the silicon. Figure 8 shows the oxidation rate constants for dry oxygen as a function of phosphorus doping level.[29] Here B/A increases substantially at high concentrations, thus reflecting the reaction-rate control, whereas B is relatively independent of concentration, thus reflecting the diffusion-limited control.

The oxidizing interface is a complicated and not fully understood region. Its high concentration of dopant provides further complications. A theoretical model has been developed[30] to explain concentration enhancement. According to the model, the high doping levels shift the position of the Fermi level, which results in enhanced vacancy concentrations. These point defects may provide reaction sites for the chemical reaction converting Si to SiO_2, thereby increasing the reaction rate.

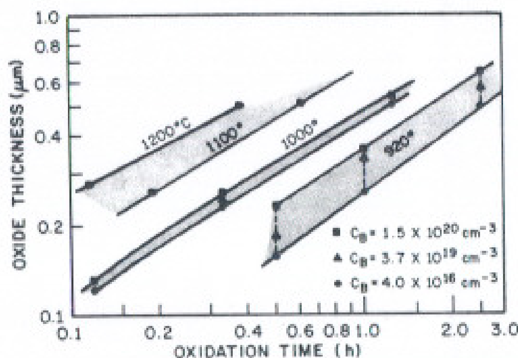

Fig. 7 Oxidation of phosphorus-doped silicon in wet oxygen (95°C H_2O) as a function of temperature and concentration. *(After Deal and Sklar, Ref. 28.)*

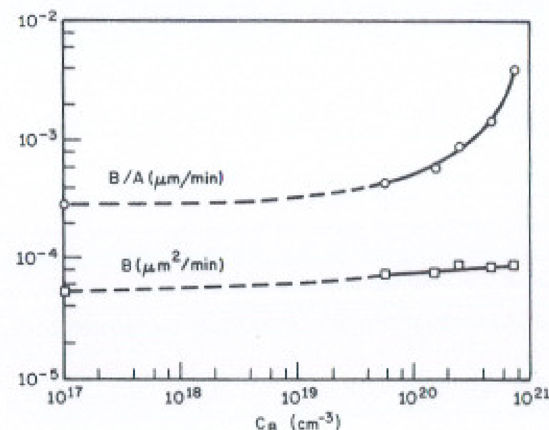

Fig. 8 Oxidation rate constants for dry oxygen as a function of phosphorus doping level at 900°C. *(After Ho et al., Ref. 29.)*

Figure 7 shows the large increase in oxidation thickness obtained for oxidation of heavily doped phosphorus in wet oxygen at lower temperatures. A dramatic example of this effect is seen in Fig. 9, which shows a bulk phosphorous-doped silicon wafer ($\sim 7 \times 10^{19}/cm^3$) after oxidation at 750°C in steam at 20-atm pressure to accelerate the kinetics. The wafer was not preferentially etched. Phosphorus dopant variations (striations), incorporated into the Czochralski crystal during solidification (see Section 1.2), appear as color variations representing oxide thickness variations. These striations clearly correspond to the concentration-enhanced oxidation of the more heavily phosphorous-doped regions in the crystal.

Halogen Certain halogen species are intentionally introduced into the oxidation ambient to improve both the oxide and the underlying silicon properties. Oxide improvements include a reduction in sodium ion contamination, an increased dielectric breakdown strength, and a reduced interface trap density. At or near the Si-SiO_2 interface, chlorine is instrumental in converting certain impurities in the silicon to volatile chlorides, resulting in a gettering effect. A reduction in oxidation-induced stacking faults is also observed. Chlorine is typically introduced into dry oxygen ambients in the form of chlorine gas, anhydrous HCl, or trichlorethylene.

Experimental results[31] for dry O_2−HCl mixtures show that HCl additions increase the oxidation rate. Typical HCl additions range from 1 to 5%. The parabolic rate constant B increases linearly with HCl additions above 1%. At 1000 and 1100°C large increases in B are initially observed. The linear rate constant B/A shows an initial increase when 1% HCl is added, but no further increase with subsequent HCl additions. The mechanisms associated with this enhanced growth rate are not fully understood. However, the generation of water upon adding HCl to dry oxygen does not account fully for the increased oxidation rate, since a similar increase occurs when chlorine[31] is added (even though no water is generated in that case).

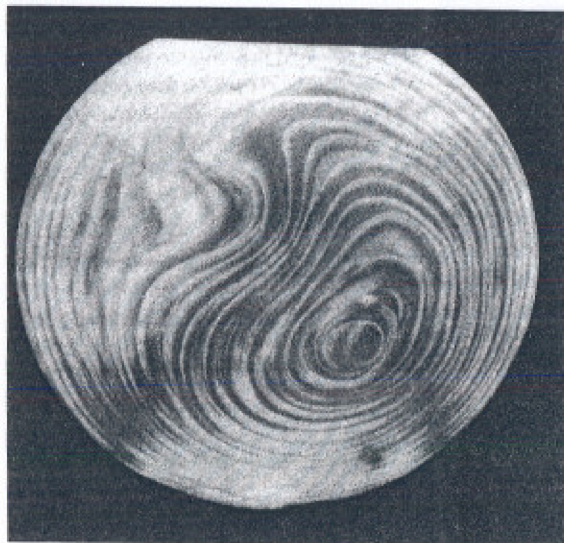

Fig. 9 Concentration-enhanced oxidation, showing dopant variations in a heavily doped phosphorus substrate.

For thermal oxidation of silicon in H_2O, adding 5 volume % HCl decreases the silicon oxidation rate by about 5%, apparently because of the reduced H_2O vapor pressure.[25] Although it is not common practice to add HCl to H_2O ambients, such addition appears to reduce impurity contamination from the oxidation system.

Thermal oxidation of silicon at 1100°C with additions of up to 1% trichlorethylene (TCE) yield oxidation rates comparable to similar concentrations of chlorine. At lower temperatures the values for O_2/TCE are larger. The mechanisms involved are complicated and not fully understood.

Finally, a word of caution. Care must be taken in handling and using the halogens mentioned since the system's metallic parts and exhaust can corrode. Additionally, high concentrations of halogens at high temperatures can pit the silicon surface.

Effect of damage on oxidation rate Determining how damage to the silicon affects the oxidation rate is not easy. To study these effects, the silicon is usually intentionally damaged by ion implantation of a nonelectrically active species (Si or A), or of a group III or V dopant. Separating damage effects from dopant effects is difficult.

Enhanced thermal oxidation of implanted silicon as a function of ion species and concentration has been studied.[32] Implanted into (100) silicon were 80-keV arsenic, 60-keV boron, 106-keV antimony, and 48-keV argon with ion doses ranging from 4×10^{14} to 1×10^{16} cm^{-2}. For wet oxidation at 900°C the maximum enhancement of the oxidation rate was a factor of 1.1 for boron, 1.3 for argon, 3.5 for antimony, and 7.5 for arsenic. The higher enhancements occurred for the higher doses. The enhancement for argon is attributed to the damage effect; for the other cases the presence of the impurity atoms certainly contributes to the enhancement. Another study[33] found a retardation effect for oxidation, following implantation of Ge, Si, and Ga into silicon. It also found an enhancement for B, Al, P, As, and Sb.

4.3 OXIDATION TECHNIQUES AND SYSTEMS

The oxidation technique chosen depends upon the thickness and oxide properties required. Oxides that are relatively thin and those that require low charge at the interface are typically grown in dry oxygen. When sodium ion contamination is of concern, $HCl-O_2$ is the preferred technique. Where thick oxides (i.e., >0.5 μm) are desired steam is used (~1 atm or an elevated presure of up to 25 atm). Higher pressure allows thick oxide growth to be achieved at moderate temperatures in reasonable amounts of time.

One-atmosphere oxide growth, the most commonly used technique, is carried out in a quartz or silicon diffusion tube with the silicon wafers held vertically in a slotted paddle (boat) made of quartz or silicon. Typical oxidation temperatures range from 800 to 1200°C and should be held to within ±1°C to ensure uniformity. In a standard procedure the wafers are cleaned, dried, placed on the paddle, and automatically inserted into an 800 to 900°C furnace, which is then ramped up to temperature. Ramping is used to prevent wafer warpage. Following oxidation, the furnace is ramped down and the wafers are removed.

Eliminating particles during oxidation is necessary to grow high-quality, reproducible oxides. In earlier procedures the paddle rested directly on the tube during insertion and withdrawal or an integrated roller paddle design was used. In either case particulates were generated. Innovative designs now use a cantilevered arrangement; the paddle is inserted into the oxidation tube in a contactless manner and then lowered onto the tube. It is removed by reversing the steps.

4.3.1 Preoxidation Cleaning

Before placing wafers in a high-temperature furnace they must be cleaned to eliminate both organic and inorganic contamination arising from previous processing steps and handling. Such contamination, if not removed, can degrade the electrical characteristics of the devices as well as contribute to reliability problems.

Particulate matter is removed by either mechanical or ultrasonic scrubbing. Immersion processing techniques were the preferred chemical cleaning methods, until the development of centrifugal spray methods which eliminate the build up of contaminants as cleaning progresses. The chemical cleaning procedure usually involves removing the organic contamination, followed by inorganic ion and atom removal.

A common cleaning procedure[34] uses a $H_2O-H_2O_2-NH_4OH$ mixture to remove organic contamination by the solvating action of the ammonium hydroxide and the oxidizing effect of the peroxide. This process can also complex some group I and II metals. To remove heavy metals a $H_2O-H_2O_2-HCl$ solution is commonly used.

This solution prevents replating by forming soluble complexes with the removed ions and is performed between 75 and 85°C for 10 to 20 minutes, followed by a quench, rinse, and spin dry.[34]

Many "optimum" cleaning procedures have evolved over the years. Reference 35 reviews the necessary considerations for optimizing the cleaning procedure for silicon wafers prior to high-temperature operations.

Modern diffusion (oxidation) furnaces are microprocessor controlled to provide repeatable sequencing, temperature control, and gas flow (mass flow control). The entire procedure previously described, from boat loading to boat withdrawal, is programmed. The microprocessor control provides a feedback loop for comparing the various parameters to the desired ones and for making the appropriate changes. For example, the actual temperature of operation may change when the gas flow is changed. Direct digital control compares this temperature to the programmed temperature and automatically makes any necessary power changes.[36]

4.3.2 Dry, Wet, HCl Dry Oxidation

Dry oxidation or HCl dry oxidation is straightforward using microprocessor-controlled equipment. The desired insertion and withdrawal rates, ramp rates, gas flows, and temperatures are all programmable. Care must be taken in handling HCl especially with the exhaust because HCl corrodes metal parts. Also remember that trace amounts of water vapor can drastically effect the oxidation rate.

Wet oxidation can be conveniently carried out by the pyrogenic technique, which reacts H_2 and O_2 from water vapor. The microprocessor controls the H_2/O_2 mixture. The pyrogenic technique assures high-purity steam, provided high-purity gases are used. If wet oxidation by the bubbler technique is used, a carrier gas is typically flowed through a water bubbler maintained at 95°C. This temperature corresponds to a vapor pressure of approximately 640 Torr.

4.3.3 High Pressure

As we saw in Eq. 14b, the parabolic rate constant B is directly proportional to C^*, the equilibrium bulk concentration in the oxide, which in turn is proportional to the partial pressure of the oxidizing species in the gas phase. Oxidation in high-pressure steam produces a substantial acceleration in the growth rate.

High-pressure oxidation of silicon is particularly attractive, because thermal oxide layers can grow at relatively low temperatures in run times comparable to typical high-temperature, 1-atm conditions. The movement of previously diffused impurities can be minimized. Low-temperature operating conditions also minimize lateral diffusion, which is of great importance as device dimensions get smaller. Another advantage is that oxidation-induced defects are suppressed (see Section 4.7). For higher-temperature, high-pressure oxidations, the oxidation time is reduced significantly.

High-pressure oxidation has been under investigation since the early 1960s.[23,37] Both experimental and production equipment are now available, along with device applications. For example, a high-speed, high-density, oxide-isolated bipolar process[38] has been described. In the MOS arena application has been successfully made to the growth of a thick-field oxide layer in a dynamic RAM.[39] The high-pressure technique is very promising and is beginning to be used more extensively.

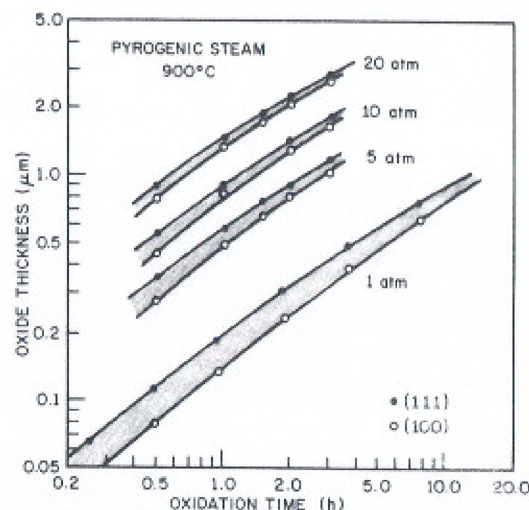

Fig. 10 Oxidation thickness versus oxidation time for pyrogenic steam at 900°C for (100) and (111) silicon and pressures up to 20 atm. *(After Razouk, Lie, and Deal, Ref. 40.)*

Figure 10 shows oxide thickness versus time data[40] for steam oxidation at various pressures and 900°C. The substantial acceleration in the oxidation rate caused by the increased pressure is apparent. In analyzing the kinetics of oxidation at elevated pressure, several complications arise such as: continuous variations in pressure during pressurization, slightly variable pressurization times, small temperature variations that occur during pressurization and during the early part of the oxidation at full pressure, varying partial pressure of steam during depressurization, and thickness variations from run to run and across a wafer. A linear-parabolic model was used to analyze the data shown in Figure 10. A linear pressure dependence[40] was observed for both the linear and parabolic rate constants. Figure 11 shows the results for the parabolic rate constant,[40] where the dotted lines represent 5, 10, 15, and 20 times the parabolic rate constant at 1 atm. The figure shows that the rate constant is proportional to pressure, and also indicates the presence of a second activation energy below 900°C. This may be related to structural changes in the oxide.[40] A typical 10-atm oxidation cycle[41] is shown in Figure 12.

Both pyrogenic and water-pumped equipment can provide steam oxidation to 25 atm pressure and 1100°C.[41] The water-pumped system alleviates the concern associated with using hydrogen at high pressure and temperature, but requires extra attention to purity since the water quality and pumping apparatus determine the steam quality. Equipment for growing dry oxides at pressures up to 700 atm is in the developmental stages.

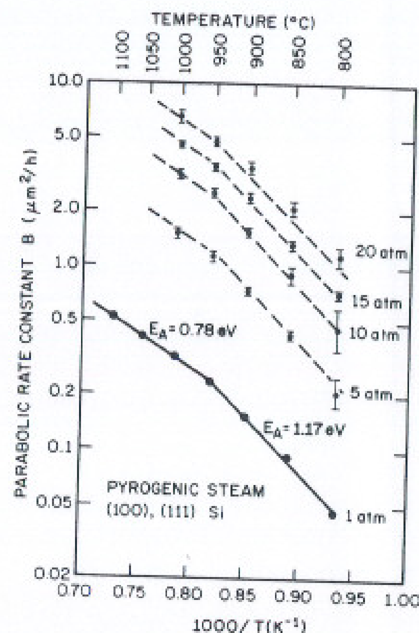

Fig. 11 Parabolic rate constant versus $1000/T$ for (100) and (111) silicon oxidized at pressures of 1, 5, 10, 15, and 20 atm in pyrogenic steam. *(After Razouk, Lie, and Deal, Ref. 40.)*

4.3.4 Plasma Oxidation

The anodic plasma-oxidation process offers the possibility of growing high-quality oxides at temperatures even lower than those achieved with the high-pressure technique. This process[42] has all the advantages associated with low-temperature processing, such as movement of previous diffusions and suppression of defect formation. Anodic plasma oxidation can grow reasonably thick oxides (on the order of 1 μm) at low temperatures (<600°C) at growth rates up to about 1 μm/h.

Plasma oxidation is a low-temperature vacuum process usually carried out in a pure oxygen discharge. The plasma is produced either by a high-frequency discharge or a DC electron source. Placing the wafer in a uniform density region of the plasma and biasing it positively below the plasma potential allows it to collect active charged oxygen species. The growth rate of the oxide typically increases with increasing substrate temperature, plasma density, and substrate dopant concentration.

The mechanisms involved with plasma oxidation are not fully understood. Uncertainty exists as to whether the oxide grows by the inward migration of oxygen species or by other, more complicated mechanisms. One model proposes that silicon and oxygen ions and/or their vacancies move across the oxide in opposite directions as a result of the applied electric field across the oxide.[43]

The beneficial effect of plasma oxidation will occur with selective oxidation

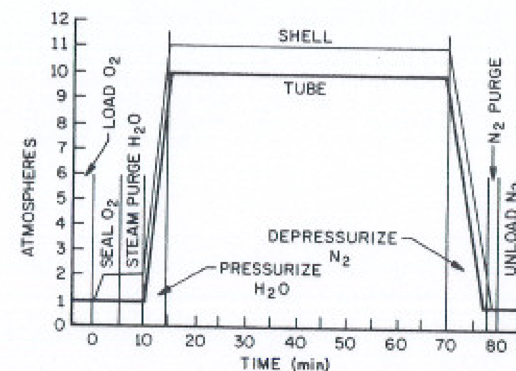

Fig. 12 Typical 10-atm steam oxidation cycle. *(After Katz et al., Ref. 41.)*

techniques (where portions of the wafer are masked against oxidation). Appropriate oxidation masks include aluminum oxide, magnesium oxide, and silicon nitride patterned by the photolithographic technique. Oxide properties, specifically the etch rate, refractive index, stress, fixed charge, interface states, and breakdown strength of plasma oxides grown at 500°C compare favorably to the properties of thermal oxides grown at 1100°C.[43–45]

4.4 OXIDE PROPERTIES

Although the literature quotes specific values for various oxide properties, it is becoming apparent that these values are affected by the experimental conditions of oxide growth. For example, the index of refraction of dry oxides[19] decreases with increasing temperature, saturating above 1190°C at an index of 1.4620. Additionally, the apparent density of oxides grown at 800°C is 3% greater than those grown[19] above 1190°C. The etch rate of thermal oxides at room temperature in buffered HF (49%) is generally quoted at about 1000 Å/min but varies with temperature and etch solution. The etch rate also varies with oxide density and thus with oxidation temperature. Measurements show that high-pressure oxides grown at 725°C and 20 atm exhibit a higher index of refraction, higher density, and slower etch rate in buffered HF than steam oxide grown at 900°C and 1 atm.[46] This difference is partially caused by the oxidation temperature effect.

For thin oxides the role of the interface in determining oxide properties is important. Unanswered questions involve the effect of lattice mismatch on oxide structure, optical properties, oxide kinetics, and oxide defects such as pinholes.

4.4.1 Masking Properties of SiO_2

A silicon dioxide layer can provide a selective mask against the diffusion of dopant atoms at elevated temperatures, a very useful property in IC processing. A predepo-

Table 7 Diffusion constants in SiO_2

Dopants	Diffusion constants at 1100°C (cm^2/s)
B	3.4×10^{-17} to 2.0×10^{-14}
Ga	5.3×10^{-11}
P	2.9×10^{-16} to 2.0×10^{-13}
As	1.2×10^{-16} to 3.5×10^{-15}
Sb	9.9×10^{-17}

sition of dopant, by ion implantation, chemical diffusion, or spin-on techniques, typically results in a dopant source at or near the surface of the oxide. During the high-temperature drive-in step, diffusion in the oxide must be slow enough with respect to diffusion in the silicon that the dopants do not diffuse through the oxide in the marked region and reach the silicon surface. The required thickness may be determined by experimentally measuring, at a particular temperature and time, the oxide thickness necessary to prevent the inversion of a lightly doped silicon substrate of opposite conductivity. A safety factor is added to this value. The impurity masking properties result when the oxide is converted into a silica impurity oxide "glass" phase.

The values of diffusion constants for various dopants in SiO_2 depend on the concentration, properties, and structure of the SiO_2. Not surprisingly quoted values may vary significantly. Table 7 lists diffusion constants for various common dopants.[47]

The commonly used n-type impurities P, Sb, and As, as well as the most frequently used p-type impurity B, all have very small oxide diffusion coefficients and are compatible with oxide masking. This is not true for gallium or aluminum (Al data not shown). Typically, oxides used for masking common impurities in conventional device processing are 0.5 to 0.7 μm thick.

4.4.2 Oxide Charges

The Si-SiO_2 interface contains a transition region, both in terms of atom position and stoichiometry, between the crystalline silicon and amorphous silica. Various charges and traps are associated with the thermally oxidized silicon, some of which are related to the transition region. A charge at the interface can induce a charge of the opposite polarity in the underlying silicon, thereby affecting the ideal characteristics of the MOS device. This results in both yield and reliability problems.

Figure 13 shows general types of charges.[48] These charges are described by $N = Q/q$ where Q is the net effective charge per unit area (coulombs/cm^2) at the Si-SiO_2 interface, N is the net number of charges per unit area (number/cm^2) at the Si-SiO_2 interface, and q is the electric charge. A brief description of the various charges follows.

Located at the Si-SiO_2 interface, interface-trapped charges Q_{it} have energy states in the silicon forbidden bandgap and can interact electrically with the underlying silicon. These charges are thought to result from several sources, including structural

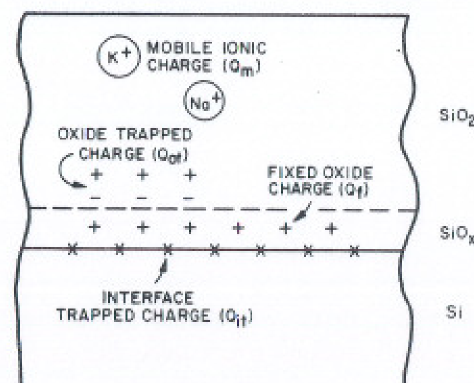

Fig. 13 Charges in thermally oxidized silicon. *(After Deal, Ref. 48.)*

defects related to the oxidation process, metallic impurities, or bond breaking processes. A low-temperature hydrogen anneal (450°C) effectively neutralizes interface-trapped charge.[48] The density of these charges is usually expressed in terms of unit area and energy in the silicon badgap (number/cm^2-eV). Capacitance-voltage (high frequency, low frequency, or quasistatic) and conductance-voltage techniques are typically used to determine the interface-trapped charges.[6] Values of $10^{10}/cm^2$-eV and lower have been observed.

The fixed oxide charge Q_f (usually positive) is located in the oxide within approximately 30 Å of the Si-SiO_2 interface. Q_f cannot be charged or discharged. Its density ranges from $10^{10}/cm^2$ to $10^{12}/cm^2$, depending on oxidation and annealing conditions as well as orientation. Q_f is related to the oxidation process itself. For electrical measurements Q_f can be considered as a charge sheet at the Si-SiO_2 interface. The value of this charge can be determined using the capacitance-voltage (C-V) analysis technique and the following equation

$$\frac{Q_f}{q} = (-V_{FB} + \phi_{MS})\frac{C_0}{q} = (-V_{FB} + \phi_{MS})\frac{\epsilon_s}{q d_0} \tag{19}$$

where V_{FB} is the flatboard voltage, ϕ_{MS} is the metal silicon work-function difference, ϵ_s is the dielectric permittivity of the semiconductor, d_0 is the oxide thickness, and C_0 is the oxide capacitance per unit area. Q_f values for (100) oriented silicon are less than those for (111) silicon. This difference is apparently related to the number of available bonds per unit area of silicon surface.

From a processing standpoint both temperature and ambient determine Q_f.[49] In an oxygen ambient, the last high-temperature treatment determines Q_f; rapid cooling from high temperatures results in low values. Inert ambient annealing also results in low Q_f, however; at low temperatures enough time must be allowed for equilibrium to be reached.

The mobile ionic charge Q_m is attributed to alkali ions, such as sodium, potassium, and lithium, in the oxide as well as to negative ions and heavy metals. The

alkali ions are mobile even at room temperature when electric fields are present. Densities range from $10^{10}/cm^2$ to $10^{12}/cm^2$ or higher and are related to processing materials, chemicals, ambient, or handling. Because of larger ionic radii and lower mobility, the heavier elements contributing to this charge drift at a slower rate than the lighter elements. Measurements can be made by using the C-V technique which involves a change in the silicon surface potential or current flow in the oxide as a result of ionic motion. Both the interface-trapped charge and oxide-trapped charge must be annealed to ensure that they do not contribute to the mobile ionic charge. Since alkali ions can be present at various places in the oxide, the MOS capacitor is subjected to a temperature-bias stress test which is compared to the standard C-V plot. The shift in flat-band voltage between the two curves allows the mobile ionic charge to be calculated. Common techniques to minimize this charge include cleaning the furnace tube in a chlorine ambient, gettering with phosphosilicate glass, and using masking layers such as silicon nitride. Although chlorine in the oxidation ambient and hence in the oxide can complex sodium, the temperatures at which this is effective are higher than the normal processing temperatures.

Oxide-trapped charge Q_{ot} may be positive or negative due to holes or electrons trapped in the bulk of the oxide. This charge is associated with defects in the SiO_2, may result from ionizing radiation, avalanche injection, or high currents in the oxide, and can be annealed out by low-temperature treatment (although neutral traps may remain).[48] Densities range from less than $10^9/cm^2$ to $10^{13}/cm^2$. Again the C-V technique can be used to measure the charge.

In addition to the earlier concerns, such as exposure of devices to ionizing radiation encountered in space flights, additional concerns arise from the newer device-processing techniques such as ion implantation, e-beam metallization, plasma or reactive-sputter etching, and e-beam or x-ray lithography.

4.4.3 Oxide Stress

Understanding the stress associated with a film is important, because high stress levels can contribute to wafer warpage, film cracking, and defect formation in the underlying Si. Room temperature measurements following thermal oxidation of silicon show SiO_2 to be in a state of compression on the surface. Stress values of 3×10^9 dynes/cm^2 are reported[50] with the stress attributed to the differences in thermal expansion for Si and SiO_2. Viscous (shear) flow of thermally grown SiO_2 occurs at temperatures as low as 960°C, evidenced by the inability of the oxide-silicon structure (oxide on one side only) to remain thermally warped above that temperature.[51] In one experiment the stress present in thermal (wet) SiO_2 during growth was measured as a function of growth temperature[52] in the range of 850 to 1030°C. Growth at 950°C and below resulted in a compressive stress of approximately 7×10^9 dynes/cm^2 in the SiO_2. This at-temperature stress value is somewhat higher than the room temperature value of 3×10^9 dynes/cm^2 given above, indicating the possibility of some stress relief during cool down. Stress-free growth at 975 and 1000°C was achieved.

During device processing, windows are cut into the oxide resulting in a complex stress distribution. At these discontinuities exceedingly high stress levels can occur.

Typically such stress would be relieved by plastic flow or other stress-relief mechanisms. The stress reduction is further accomplished by shear components which average the load over adjacent areas.[50]

The possibility of structural damage in the silicon is very real. Shear stresses at the interface are comparable to the values of compressive stress given above.[51] These shear stresses are substantially higher than the values of 3.2×10^7 dynes/cm^2 to 4.3×10^7 dynes/cm^2 given for the critical stress of shear flow for silicon at 800°C.[53] This leads to the possibility of plastic deformation in the silicon. The deleterious effect of structural damage in the silicon (particularly when decorated with impurities) on junction leakage and on other device properties is well documented. Additionally, viscous shear flow has been related to hole traps at the interface.

4.5 REDISTRIBUTION OF DOPANTS AT INTERFACE

When silicon is thermally oxidized, an interface is formed separating the silicon from the SiO_2. As oxidation proceeds this interface advances into the silicon. A doping impurity (initially present in the silicon) will redistribute at the interface until its chemical potential is the same on each side of the interface. This redistribution may result in an abrupt change in impurity concentration across the interface. The ratio of the equilibrium concentration of the impurity (dopant) in silicon to that in SiO_2 at the interface is called the equilibrium segregation coefficient. (Note: In some literature an inverse definition is used, so care must be taken in using published values.) The experimentally determined segregation coefficient may differ from the equilibrium segregation coefficient. This will primarily be determined by the chemical potential differences and the kinetics of redistribution at the interface.

Two additional factors that influence the redistribution process are the diffusivity of the impurity in the oxide (if large, the dopant can diffuse through the oxide rapidly, affecting the profile near the Si-SiO_2 interface) and the rate at which the interface moves with respect to the diffusion rate. Figure 14 shows four different possibilities of impurity segregation.[54]

The segregation coefficient determined experimentally is called the effective or interface segregation coefficient. It is particularly important to understand the concentration profile at the interface since electrical characteristics are affected. In extreme cases inversion can occur.

Typically, to determine the segregation coefficient experimentally, a model for diffusion has been formulated, diffusion profiles experimentally determined in the silicon, and a segregation coefficient chosen to force the data to fit the model. Direct determination of the segregation coefficient is possible using the secondary-ion mass spectrometry (SIMS) technique to obtain concentration values in the oxide and in the silicon.

Most of the effort in segregation coefficient determination has been related to boron. The segregation coefficient, as defined above, increases with increasing temperature, and is orientation dependent with values for (100) orientation being greater than for (111) orientation. Reported coefficients[55–57] are generally 0.1 to approxi-

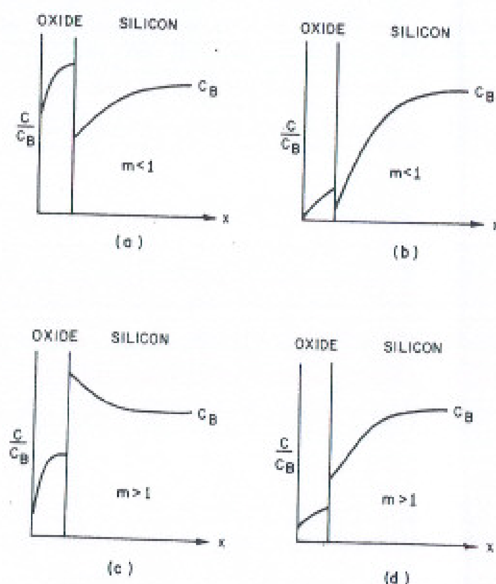

Fig. 14 Impurity segregation at the Si-SiO_2 interface resulting from thermal oxidation. (a) Diffusion in oxide slow (boron); (b) diffusion in oxide fast (boron-H_2 ambient); (c) diffusion in oxide slow (phosphorus); and (d) diffusion in oxide fast (gallium). *(After Grove, Leistiko, and Sah, Ref. 54.)*

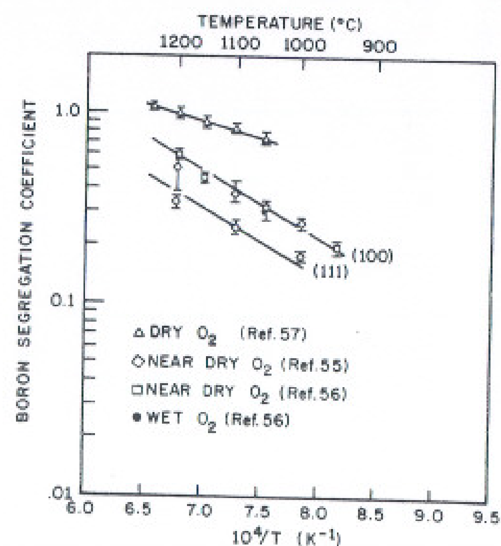

Fig. 15 Boron segregation coefficient as a function of temperature for dry, near dry, and wet oxidations. *(After Fair and Tsai, Ref. 56.)*

mately 1.0 over the temperature range 850 to 1200°C, although values greater than 1 have been obtained in special cases.[56] Figure 15 shows the results of some boron segregation determinations. Because very small amounts of moisture can greatly affect the segregation coefficient, a distinction must be made between dry, near dry, and wet oxidations. A "dry oxidation" containing even 20-ppm moisture exhibits a segregation coefficient similar to that of wet oxidation. The data in Fig. 15 shows that "near dry" oxidation (obtained in a furnace without special drying precautions) and wet oxidation give virtually identical segregation coefficients. Larger segregation coefficient values are obtained when special drying precautions are taken.[57] Additionally, boron implanted through oxide even when subsequent oxidations are performed in ambients with trace amounts of H_2O has segregation coefficients equal to those for dry O_2. These effects are particularly important at lower temperatures. For example, at 900°C the surface concentration following a "near dry" oxidation is approximately one-half that of pure dry oxidation.[56] Quoted effective segregation coefficients (m_{eff}) for boron in silicon are[56]

1. Pure dry O_2, orientation independent

$$m_{\text{eff}} = 13.4 \exp \frac{-0.33 \text{ eV}}{kT} \tag{20}$$

2. Near dry or wet O_2

$$m_{111(\text{eff})} = 65.2 \exp \frac{-0.66 \text{ eV}}{kT} \tag{21}$$

$$m_{100(\text{eff})} = 104.0 \exp \frac{-0.66 \text{ eV}}{kT} \tag{22}$$

For phosphorous, arsenic, and antimony, where the dopant segregates into the silicon (pile-up), segregation coefficient values of approximately 10 are usually quoted,[54] although higher values (up to 800 at 1050°C) have been determined for arsenic. With gallium, which diffuses rapidly in the oxide, a value of approximately 20 is given.[54]

4.6 OXIDATION OF POLYSILICON

Polycrystalline silicon has been used in IC technology to provide conducting lines between devices and gates. Thermal oxidation of polycrystalline silicon provides electrical isolation which can be employed as an interlevel dielectric for multilayer structures. An understanding of the oxidation mechanisms is necessary since device reliability depends on the quality of the oxide. Various parameters of polycrystalline silicon including growth method, growth temperature, doping level, grain size, and morphology have been studied with respect to oxidation rate and oxide properties, such as electrical conductivity and breakdown. Typically, comparisons are made with oxides grown on single-crystal silicon.

In one study,[58] using CVD doped and oxidized polycrystalline films, the atmospheric-pressure polysilicon (deposited at 960°C) oxidized at the same rate as low-presure polysilicon (deposited at 625°C). However, a substantial difference with respect to single-crystal silicon was observed. At moderate doping levels, the electrically active carrier concentration at the surface controlled the oxidation rate. While the total amount of dopant introduced into polysilicon and single-crystal samples was the same, the dopant diffused more deeply in the polysilicon reducing the oxidation rate with respect to single-crystal silicon. This result should not be too surprising in light of our previous discussion of concentration-enhanced oxidation. Following a phosphorus "predeposition," having 70-Ω/□ sheet resistance and 850°C steam oxidation, oxide thickness values of approximately 3000 to 3200 Å on polysilicon, approximately 3850 Å on (100) single crystal, and approximately 4250 Å on (111) single crystal were obtained.[58] The ratio of polysilicon-consumed oxidation to oxide grown was about the same as for single-crystal silicon (0.45).

In another study,[59] using CVD (at 625°C) undoped polysilicon and lightly doped single-crystal silicon, the oxidation rate increased in the following order: (100), (111), polysilicon, and (110). These observations are consistent with the transmission electron microscope determination that the polysilicon was oriented between (111) and (110). For heavily phosphorous-doped polysilicon, the parabolic rate constant is saturated at concentrations greater than 2×10^{20} cm^{-3} while the linear rate constant continues to increase.

If the oxidation rate of polysilicon depends on the random orientation of the grains, which is true in the surface or reaction-controlled region, then a surface roughening would be expected. Surface roughening, however, is not as pronounced for oxidations at higher temperatures where diffusion control is predominant. Transmission electron microscope results[60] show that the oxide exhibits thickness undulations coincident with previous grain boundaries. The oxide is thinner over grain boundaries by approximately 25% and forms intergranularly in addition to forming on the surface. For higher-temperature oxidations, the thickness undulations are less severe because the oxide and silicon can flow and the reaction can enter the diffusion-controlled region.

Device reliability may be affected when the oxide is removed to open the contacts to the polysilicon; the oxide in the intergranular regions may also be removed unintentionally. Subsequent metallization can form a conducting path along the exposed regions between the grains in the polysilicon, and electrical shorts.[60]

4.7 OXIDATION-INDUCED DEFECTS

4.7.1 Oxidation-Induced Stacking Faults

Thermal oxidation of silicon can produce stacking faults lying on (111) planes. These planar faults are structural defects in the silicon lattice that are extrinsic in nature and are bounded by partial dislocations. The growth mechanism generally invoked involves the coalescence of excess silicon atoms in the silicon lattice on nucleation

sites such as defects grown in during crystal growth, surface mechanical damage present prior to oxidation, chemical contamination, or defects referred to as saucer pits or hillocks. As a result of the oxidation process, excess interstitial silicon is present near the Si-SiO_2 interface. A small fraction of these silicon atoms flow into the bulk silicon. The silicon interstitial supersaturation in the silicon determines the stacking fault growth rate.[61] An alternative explanation involves a decreased vacancy concentration in the silicon near the Si-SiO_2 interface.

The deleterious nature of oxidation-induced stacking faults is well known. Examples include degraded junction characteristics in the form of increased reverse leakage current, and storage time degradation in MOS structures. These problems occur when the stacking faults are electrically active as the result of being decorated with impurities, typically heavy metals. The decoration occurs both on the stacking fault itself and on the bounding dislocations. The dislocations, in particular, are favorable clustering sites because they represent a disarrayed high-energy region in the lattice. Diffusing impurity atoms prefer to reside in such a region because they distort the lattice less here than in the perfect lattice; that is, the high-energy region is energetically more favorable.

The growth of oxidation-induced stacking faults is a strong function of substrate orientation, conductivity type, and defect nuclei present. Observations show that the growth rate is greater for (100) than (111) substrates. Additionally, the density is greater for n-type conductivity than for p-type conductivity. Figure 16 shows that stacking fault length is a strong function of oxidation temperature.[62] The activation energy in the growth region is 2.3 eV independent of surface orientation and ambient (dry or wet). In the retrogrowth temperature range, stacking faults initially grow and then begin to shrink as oxidation proceeds. Typically the distribution of surface stacking fault lengths is very tight, except for an anomalous few percent which exhibit substantially greater lengths. Shorter-length stacking faults are usually bulk-nucleated stacking faults intersecting the surface. The length to depth ratio of the surface-oxidation stacking fault is approximately 3 to 10.

The curves in Fig. 16 clearly show two regions: a growth region and a retrogrowth region. In the retrogrowth region, stacking fault formation is suppressed while preexisting stacking faults shrink. The addition of HCl to the ambient can also suppress stacking fault formation.[63] Additional observations show, for comparable oxide thickness, shorter stacking faults are grown (in the growth region) when the oxidation temperature is lower. Indeed even for oxides as thick as 1 μm, stacking fault formation is completely suppressed when the temperature is reduced below 950°C.[64] Shrinkage of preexisting stacking faults can also be accomplished by high-temperature inert ambient heat treatment, N_2 for example, with an activation energy of approximately 5 eV (which is almost equal to the activation energy of silicon self-diffusion). This indicates that the shrinkage is probably related to the diffusion of silicon atoms.

Experimental observations show that at comparable temperature and time, the oxidation stacking fault length is greater for steam ambients than for dry ambients. This suggests that the oxidation rate strongly influences the point-defect mechanism

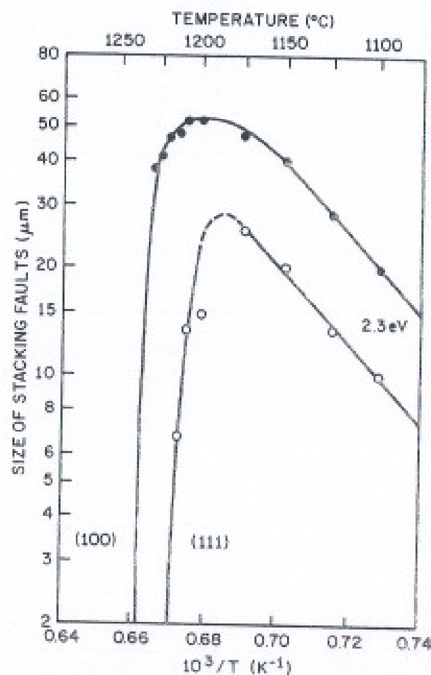

Fig. 16 Growth of oxidation-induced stacking faults versus temperature; for 3 h of dry oxidation. *(After Hu, Ref. 62.)*

responsible for stacking fault growth. Equation 23 is a proposed model[61] in which the oxidation rate is the controlling parameter in oxidation stacking fault length.

$$\frac{dl}{dt} = K_1 \left[\frac{dT_{ox}}{dt} \right]^n - K_2 \tag{23}$$

where l is the stacking fault length, T_{ox} is the oxide thickness, t is the time, n is the power dependence, K_1 is related to the growth mechanism and defect generation at the Si-SiO_2 interface, and K_2 is related to the retrogrowth mechanism. Applying this equation to experimental data gives values for n, K_1, and K_2. A 0.4th power dependence is observed.[61] This less-than-linear dependence of oxidation stacking fault growth rate on the oxidation rate means that smaller stacking faults will result for a higher oxidation rate at the same temperature for the same oxide thickness. This, of course, is the case with high-pressure oxidation where the oxidation rate is increased. Figure 17 shows an experimental result for a 950 to 1100°C temperature range at both 1- and 6.4-atm pressure.[64] The above results confirm the proposed model. Additional results[65] at 700°C and 20-atm pressure show complete stacking fault suppression for all thicknesses studies (up to 5 μm). Preexisting stacking faults tend to grow during

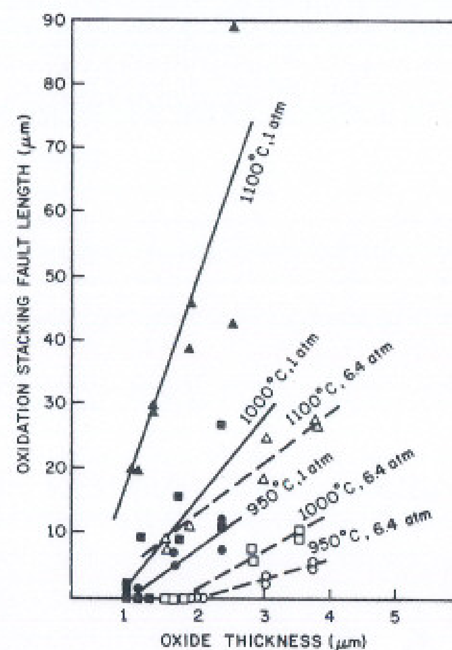

Fig. 17 Length of oxidation-induced stacking faults versus oxide thickness for 1-atm and 6.4-atm steam oxidations. *(After Tsubouchi, Miyoshi, and Abe, Ref. 64.)*

this high-pressure, low-temperature oxidation. However, the net length of the stacking fault is reduced by the consumption of silicon.

4.7.2 Oxide Isolation Defects

Selective oxidation of silicon represents an important process in IC processing. For VLSI, oxide isolation is preferred to junction isolation. Stress along the edge of an oxidized area especially in recessed oxides (that is, where the silicon has been trenched prior to oxidation to produce a reasonably planar surface) may produce severe damage in the silicon. Such defects result in increased leakage in nearby devices. The stress generated by the growing oxide, whose volume is over twice that of the consumed silicon, must be relieved without damaging the silicon. Various parameters have been examined for recessed isolation processes with the conclusion that the oxidation temperature must be sufficiently high to allow the stress in the oxide to be relieved by viscous flow. Temperatures (around 950°C) will prevent stress-induced defect formation in a recessed structure (recess approximately 1 μm and oxide growth approximately 2.2 μm). This critical temperature correlates well with that for stress-free growth in oxides at 1 atm.

4.8 SUMMARY AND FUTURE TRENDS

The ability to mathematically describe the oxidation process reasonably well in its simplest form has been demonstrated. Our understanding of the oxidizing species and the point-defect mechanisms in the vicinity of the oxidizing interface is still evolving. We can determine experimentally the effect of impurity species, dopant concentration, and orientation on the oxidation kinetics, but are somewhat less able to explain some of the mechanisms involved.

An understanding of oxide charge is necessary in order to fabricate highly reliable devices. This is particularly important with the new processing techniques used for VLSI fabrication. An understanding of how to form oxides without damaging the underlying silicon is necessary when fabricating advanced structures, such as dielectrically isolated devices that may require thick recessed oxides. Oxide viscosity is a first-order effect, and oxidation temperatures above 950°C minimize stress-related defect formation.

Polycrystalline silicon usage has become increasingly important and has attracted more study recently both in its formation and oxidation. The polysilicon deposition technique, polysilicon grain size, orientation, and doping level all affect oxidation. Formation of oxide in intergranular regions and its removal when contacts to the polysilicon are opened leads to the possibility of electrical shorts during metallization.

The impact of continually shrunken vertical and lateral dimensions, tighter design rules, and lower-temperature processing cannot be overlooked in future research. The recent availability of commercial high-pressure oxidation equipment allows thick oxides to be grown at low to moderate temperatures. As an added bonus, suppression of oxidation-induced stacking is obtained. This technique has not been exploited to any great extent, but more utilization is undoubtedly in the offing.

A low-temperature technique for growing reasonably thick oxides ($\sim$1 µm in 1 h), the anodic plasma-oxidation technique, offers vast potential. The low-temperature processing suppresses defect formation and minimizes movement of previous diffusions. Oxide properties are comparable to those of thermally grown oxides. Uses should proliferate when commercial equipment becomes available.

The prevention of the bird's beak during selective oxidation is another area which is receiving much attention and has a potentially big payoff. Bird's beak is associated with the thin "pad" oxide necessary to prevent defect formation. The oxide is between the silicon and masking nitride layer and results from the diffusion of oxygen and growth of SiO_2. Success has been demonstrated when the silicon is selectively trenched, processed so that nitride is present on the trench sidewall, and subsequently oxidized.[66] Encouraging results have also been obtained with the anodic plasma-oxidation technique for nonrecessed oxides.[43]

Oxide requirements on advanced structures are changing. As discussed earlier, these requirements range from highly reliable thin oxides to thick isolation oxides that can be grown at moderate temperatures. Renewed emphasis on oxidation techniques, such as high-pressure and plasma oxidation, has occurred. It is inevitable that further advances will be made in growth techniques, processing schemes, and understanding of oxidation mechanisms.

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4.9 PROBLEMS

1 Show from the densities and molecular weights of Si and SiO_2 that a layer of silicon of thickness $0.45\ d_0$ is consumed when a SiO_2 layer of thickness d_0 is formed. Use density values of 2.27 gm/cm^3 for SiO_2 and 2.33 gm/cm^3 for Si.

2 Show that in Eq. 14, $d_0^2 + Ad_0 = B(t + \tau)$ reduces to $d_0^2 = Bt$ for long times and to $d_0 = B/A\,(t + \tau)$ for short times.

3 (a) Show that in Eq. 14, $d_0^2 + Ad_0 = B(t + \tau)$ can be used graphically to obtain an equation describing the oxidation rate.

(b) Generate such a plot for the 1100°C oxidation data of Fig. 5. Use $\tau = 0$ and (100) orientation to obtain rate constants. Compare your results to those of Fig. 3.

4 Using Eq. 14 and Table 1, how long will it take to grow 2.0 μm of SiO_2 at 920°C and 25-atm steam pressure?

5 Define a set of conditions to minimize the chance of inverting the surface of an n-type substrate (containing a boron diffusion) when oxidizing the wafer.

6 List possible ways of growing an initial oxide on a substrate without forming oxidation-induced stacking faults.

7 Solve Eq. 14 for oxide thickness as $f(t, \tau, A, B)$.

8 Make use of the equation derived in Problem 7, and the data in Tables 1 and 2, to generate oxide thickness versus time curves for wet and dry oxidations at 1100°C. Assume $\tau = 0$.

9 Generate a model showing possible interface reaction and point-defect fluxes at the interface.

10 Devise a processing scheme to generate selectively a planar recessed oxide in silicon. Show how you might prevent lateral oxidation during the oxide growth.

6 For a median life of 4.0×10^6 h and a σ of 1.3;

(a) What fraction of devices will have failed after 10 years of use at 70°C?

(b) If 100 of these devices are used in a system, what fraction of the systems will have failed in 10 years? (Hint: Use the Poisson approximation to the binomial probability, Eq. 4, that no failed devices are found in a given system.)

(c) What is the expected fraction of failed devices after 10 years of operation using the lower limit for the median life of 1.8×10^6 h?

(d) What is the expected fraction of failed systems?

(e) What is the expected fraction of failed devices and systems after 10 years of operation if the system is operated at 50°C where the expected mean life is 4.0×10^7 h?

7 Twenty sample devices from another production lot of the same devices as in the previous problems were evaluated at an aging temperature of 150°C. Some of the devices in this lot were believed to have been improperly processed and contaminated with sodium. These 20 devices were tested after 2, 4, 8, . . . , and 4096 h of aging. Failures were found at the following times: 32, 64 (three failures), 128, 512, 1024 (two failures), 2048 (three failures), and 4096 (two failures) h. Plot the failure distributions on log-normal plotting paper.

(a) Estimate from the inflection point of the failure distribution the fraction of contaminated or sport devices in the population.

(b) Separate the devices into sport and normal devices. Replot the failure data to determine the median life and σ of each population.

8 Assume that the sodium-contaminated sport devices comprise 25% of the population, that the median life at 150°C is 60 h, the σ is 0.7, and the activation energy is 1.0 eV. Assume that the main population has a median life at 150°C of 4800 h, a σ of 1.3, and an activation energy of 1.10 eV.

(a) Plot the failure rate of the devices as a function of time in use at a temperature of 70°C for devices used as produced.

(b) Would a 150-h burn-in at 150°C provide an effective method of reducing the failure rate of these devices during normal operation at 70°C?

APPENDIX

A

PROPERTIES OF SILICON (at 300 K)

Properties	Si
Atoms/cm^3	5.0×10^{22}
Atomic weight	28.09
Breakdown field (V/cm)	$\sim 3 \times 10^5$
Crystal structure	Diamond
Density (g/cm^3):	
Solid	2.33
Liquid (1412°C)	2.53
Dielectric constant	11.9
Effective density of states in conduction band, N_C (cm^{-3})	2.8×10^{19}
Effective density of states in valence band, N_V (cm^{-3})	1.04×10^{19}
Effective mass, m^*/m_0:	
Electrons	$m_l^* = 0.98$, $m_t^* = 0.19$
Holes	$m_{lh}^* = 0.16$, $m_{hh}^* = 0.49$
Electron affinity (V)	4.05
Energy gap (eV)	1.12
Heat capacity (cal/g-mol-°C):	
Solid	4.78
Liquid (1412°C)	6.76
Index of refraction	3.42
Intrinsic carrier concentration (cm^{-3})	1.45×10^{10}
Intrinsic Debye Length (μm)	24
Intrinsic resistivity (Ω-cm)	2.3×10^5
Lattice constant (Å)	5.43095

Properties	Si
Linear coefficient of thermal expansion, $\Delta L / L \Delta T$ (°C^{-1})	2.6×10^{-6}
Melting point (°C)	1412
Minority-carrier lifetime (s)	2.5×10^{-3}
Mobility (drift) (cm^2/V-s):	
μ_n (electrons)	1500
μ_p (holes)	475
Optical phonon energy (eV)	0.063
Phonon mean free path λ_0 (Å):	
Electrons	76
Holes	55
Poisson's ratio	0.42
Specific heat (J/g-°C)	0.7
Thermal conductivity (W/cm-°C):	
Solid	1.5
Liquid (1412°C)	4.3
Thermal diffusivity (cm^2/s)	0.9
Torsion modulus (kg/mm^2)	4050
Vapor pressure (Pa)	1 at 1650°C 10^{-6} at 900°C
Young's modulus (kg/mm^2)	10,890

APPENDIX

B

LIST OF SYMBOLS

Symbol	Description	Unit
a	Lattice constant	Å
$\mathscr{B}$	Magnetic induction	Wb/m^2
c	Speed of light in vacuum	cm/s
C	Capacitance	F
D	Electric displacement	C/cm^2
D	Diffusion coefficient	cm^2/s
E	Energy	eV
E_F	Fermi energy level	eV
E_g	Energy bandgap	eV
$\mathscr{E}$	Electric field	V/cm
$\mathscr{E}_m$	Maximum field	V/cm
f	Frequency	Hz
h	Planck's constant	J-s
$h\nu$	Photon energy	eV
I	Current	A
J	Current density	A/cm^2
k	Boltzmann constant	J/K
kT	Thermal energy	eV
L	Length	cm or μm
m_0	Electron rest mass	kg
m^*	Effective mass	kg
$\bar{n}$	Refractive index	
n	Density of free electrons	cm^{-3}
n_i	Intrinsic density	cm^{-3}
N	Doping concentration	cm^{-3}
N_A	Acceptor impurity density	cm^{-3}
N_D	Donor impurity density	cm^{-3}

Symbol	Description	Unit
p	Density of free holes	cm^{-3}
P	Pressure	N/m^2
q	Magnitude of electronic charge	C
Q_{it}	Interface-trap density	$charges/cm^2$
R	Resistance	Ω
t	Time	s
T	Absolute temperature	K
v	Carrier velocity	cm/s
v_s	Saturation velocity	cm/s
V	Voltage	V
V_{bi}	Built-in potential	V
V_B	Breakdown voltage	V
W	Thickness	cm or μm
x	x direction	
∇T	Temperature gradient	K/cm
ϵ_0	Permittivity in vacuum	F/cm
ϵ_s	Semiconductor permittivity	F/cm
ϵ_i	Insulator permittivity	F/cm
ϵ_s / ϵ_0 or ϵ_i / ϵ_0	Dielectric constant	
τ	Lifetime or decay time	s
θ	Angle	rad
λ	Wavelength	μm or Å
ν	Frequency of light	Hz
μ_0	Permeability in vacuum	H/cm
μ_n	Electron mobility	$cm^2/V\text{-}s$
μ_p	Hole mobility	$cm^2/V\text{-}s$
ρ	Resistivity	Ω-cm
ϕ	Barrier height or imref	V
ϕ_m	Metal work function	V
ω	Angular frequency ($2\pi f$ or $2\pi\nu$)	Hz
Ω	Ohm	Ω

APPENDIX
C

INTERNATIONAL SYSTEM OF UNITS

Quantity	Unit	Symbol	Units
Length	meter	m	
Mass	kilogram	kg	
Time	second	s	
Temperature	kelvin	K	
Current	ampere	A	
Frequency	hertz	Hz	1/s
Force	newton	N	$kg\text{-}m/s^2$
Pressure	pascal	Pa	N/m^2
Energy	joule	J	N-m
Power	watt	W	J/s
Electric charge	coulomb	C	A-s
Potential	volt	V	J/C
Conductance	siemens	S	A/V
Resistance	ohm	Ω	V/A
Capacitance	farad	F	C/V
Magnetic flux	weber	Wb	V-s
Magnetic induction	tesla	T	Wb/m^2
Inductance	henry	H	Wb/A

APPENDIX
D
PHYSICAL CONSTANTS

Quantity	Symbol	Value
Angstrom unit	Å	$1\text{Å} = 10^{-1}$ nm $= 10^{-4}$ μm $= 10^{-8}$ cm $= 10^{-10}$ m
Avogadro constant	N_{AVO}	6.02204×10^{23} mol^{-1}
Bohr radius	a_B	0.52917 Å
Boltzmann constant	k	1.38066×10^{-23} J/K (R/N_{AVO})
Elementary charge	q	1.60218×10^{-19} C
Electron rest mass	m_0	0.91095×10^{-30} kg
Electron volt	eV	1 eV $= 1.60218 \times 10^{-19}$ J $= 23.053$ kcal/mol
Gas constant	R	1.98719 cal mol^{-1} K^{-1}
Permeability in vacuum	μ_0	1.25663×10^{-8} H/cm $(4\pi \times 10^{-9})$
Permittivity in vacuum	ϵ_0	8.85418×10^{-14} F/cm $(1/\mu_0 c^2)$
Planck constant	h	6.62617×10^{-34} J-s
Reduced Planck constant	$\hbar$	1.05458×10^{-34} J-s $(h/2\pi)$
Proton rest mass	M_p	1.67264×10^{-27} kg
Speed of light in vacuum	c	2.99792×10^{10} cm/s
Standard atmosphere		1.01325×10^{5} N/m^2
Thermal voltage at 300 K	kT/q	0.0259 V
Wavelength of 1-eV quantum	λ	1.23977 μm

INDEX

AC discharge, 314
Accelerated testing, 624
Activation energy, 56, 99, 108, 109, 120, 138, 144, 161, 177, 183, 244, 247, 328, 370, 413, 626, 631
Aerial image, 413
Alignment sequence, 491
α-particle, 584, 635
$AlCl_3$, 340
Al-Cu alloys, 341, 364, 369
$Al_xGa_{1-x}As$, 51
$Al\text{-}Pd_{80}W_{20}\text{-}Si$, 368
$Al\text{-}Pt_{10}Cr_{90}\text{-}Si$, 368
Al-Si alloys, 341, 372
Aluminum (Al), 77, 82, 145, 149, 340, 355–357, 360, 361, 368, 369, 373, 377, 380, 428, 440, 465, 475, 513, 521, 525, 555, 558, 583, 633
Aluminum alloys, 347, 356
Aluminum nitride, 124
Aluminum oxide (Al_2O_3), 124, 366, 431, 577
Aluminum spikes, 367
Ambient control, 28
Ambient gettering, 258
Amorphous polysilicon, 105
Amplitude, 412
Angle of incidence, 321
Anisotropic etching, 305, 330, 364
Anisotropy of growth, 70
Annealing, 242, 252
Antimony (Sb), 23, 77, 149, 154, 159, 193, 205, 212, 259, 400, 452, 527
Area defect, 15, 17
Arrival angle, 112
Arsenic (As), 59, 66, 67, 77, 149, 154, 159, 193, 197, 200, 203–205, 209, 211, 220, 231, 236, 248, 253, 259, 386–388, 391, 393, 400, 452, 454, 457, 463, 471, 485, 521, 522, 524, 527, 528, 530
  intrinsic diffusivities of, 193
Arsenic clustering model, 197
Arsine (AsH_3), 58, 62, 66, 95, 98
Atomistic diffusion models, 170
Au (*see* Gold)
Auger electron spectroscopy (AES), 520
Autodoping, 56, 59, 60, 70, 82, 87, 390
Average failure rate, 620
Average ion velocity, 235

Backward difference method, 407
Ball-wedge bonding, 555
Bandgap narrowing effect, 202
Barrel susceptor, 62
Base formation, 453
BCl_3, 66
Beryllia (BeO) modules, 572
Bethe energy loss rate, 418
B_2H_6 (*see* Diborane)
BF_2, 220, 253, 255, 485, 489
Bias, 304
Binomial distribution, 605
Bipolar technology, 65, 448
Bipolar transistor, 1, 9, 169, 189, 201, 445, 446, 448–461, 494
Bird's beak, 405, 452, 461, 472
Boltzmann-Matano analysis, 176
Boltzmann transport equation, 391
Bonding, 380
Boron (B), 14, 18, 32, 77, 105, 145, 149, 154, 158, 193, 199, 201, 205, 209, 210, 213, 220, 228, 231, 235, 240, 242, 244, 245, 247, 248, 259, 390, 394, 400, 401, 440, 451, 463, 469, 485, 488, 490, 521, 528
  intrinsic diffusivity of, 193
Boro-phosphosilicate glass, 124

Appendix A

Table A.1: Physical constants

Symbol	Description	Unit	Value
N_{Si}	specific volume of silicon	atoms / cm^3	5×10^{22}
N_{SiO_2}	specific volume of SiO_2	molecules/ cm^3	2.2×10^{22}
γ	ratio of specific volume of silicon to oxide		2.27
β	# of oxidant molecules reacting with unit volume of Si	molecules/ cm^3	5×10^{22} for O_2(g) 1×10^{23} for H_2O(g)