L12

L#12

(1)

VITERBI DECODING CONSIDERATIONS

WE SAID THAT TO AVOID HAVING A LARGE PATH MEMORY (HOLDING THE TRELLIS INFORMATION) WE HAVE FIXED LENGTH HISTORY OF 4 OR 5 TIMES THE CONSTRAINT LENGTH.

THE AMOUNT OF PATH MEMORY REQUIRED IS

$$u = h\,2^{K-1}; \quad h = 4K \text{ -OR- } 5K$$

u - REQUIRED PATH MEMORY
h - LENGTH OF BIT PATH HISTORY PER STATE
K - CONSTRAINT LENGTH.

SINCE THE COMPLEXITY OF VITERBI DECODING IS DIRECTLY PROPORTIONAL TO THE NUMBER OF STATES IN THE TRELLIS, THE DECODER BE-COME IMPRACTICAL FOR $K \geq 10$.

CHIPSETS FOR VITERBI DECODING ARE AVAILABLE FROM A NUMBER OF SEMICONDUCTOR MANUFACTURERS

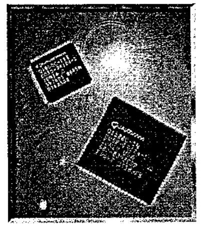
— SEE FOLLOWING TWO PAGES

(2)

QUALCOMM | ASIC PRODUCTS

Viterbi/Trellis Decoders

Q1900 Viterbi/Trellis Decoder



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Forward Error Correction (FEC) improves the bit error rate (BER) performance of power-limited and/or bandwidth-limited channels by adding structured redundancy to the transmitted data. The type of additive noise experienced on the channel determines the class of FEC used on the channel. Tree codes are used for channels with Additive White Gaussian Noise (AWGN) and block codes are used for channels with additive burst noise. The Q1900 is based on a k=7 Viterbi decoder tree code, optimizing performance over channels with AWGN. The Q1900 supports encoding and decoding for Viterbi and Trellis Modes of operation. The Viterbi Mode is typically used for systems that are power-limited but not bandwidth-limited. The standard modulation types are Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK). Trellis Mode is typically used for systems that are both power-limited and bandwidth-limited. The standard modulation types are 8-PSK and 16-PSK.

The encoders are both based on a k=7 convolutional encoder and the decoders are both based on a k=7 Viterbi decoder.

The Viterbi Mode supports four code rates: 1/3, 1/2, 3/4 and 7/8. Additional code rates can be supported with external circuitry. The Viterbi Mode also supports built-in phase synchronization for standard BPSK, QPSK, and Offset Quadrature Phase Shift Keying (OQPSK) modulation techniques. Either 1 bit hard-decision or 3 bit soft-decision input data is supported. The Viterbi Mode also includes two powerful built-in techniques for monitoring synchronization status as well as performing channel BER measurements.

The Trellis Mode supports two codes rates: 2/3 for 8 PSK and 3/4 for 16 PSK. The Trellis Mode also supports built-in phase synchronization for 8-PSK and 16-PSK. The Viterbi and Trellis Modes include a processor interface to facilitate control and status monitoring functions while keeping device pinout to a minimum.

The Q1900 is packaged in an 84-pin PLCC package or a 100-pin VTQFP package and is implemented in fully static CMOS logic to reduce power consumption. It also uses fully parallel circuit architecture to negate the requirement for a higher speed computation clock.

The Q1900 is well suited for many commercial satellite communication networks, including INMARSAT and INTELSAT. The low-cost and high performance of the Q1900 make it ideal for FEC requirements in systems such as direct broadcast satellites (DBS), microwave point-to-point data links, very small aperture terminals (VSAT), digital modems, digital video transmission systems, high-speed data modems and military and NASA communication systems.

ASIC Home | Download Literature

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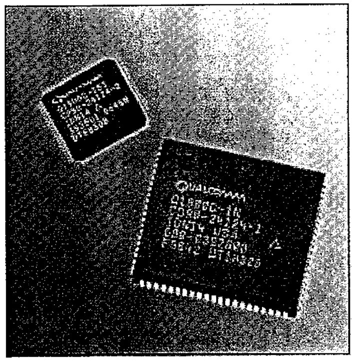
Q1900

VITERBI/TRELLIS DECODER



$16.00 USD PER PIECE (FOR 1000+ OFF. QUANTITIES)

FEATURES

- Viterbi Mode Rates 1/3, 1/2, 3/4 and 7/8
- Trellis Mode Rates 2/3 and 3/4
- Full Duplex Encode and Decode in Both Viterbi and Trellis Modes
- Large Coding Gains at Eb/No of 10^{-5}
  - 5.5 dB for Rate 1/3 Viterbi Decoding
  - 5.2 dB for Rate 1/2 Viterbi Decoding
  - 3.2 dB for Rate 2/3 Trellis Decoding
  - 3.1 dB for Rate 3/4 Trellis Decoding
- Automatic Phase Synchronization for BPSK and QPSK in Viterbi Mode and for 8-PSK and 16-PSK in Trellis Mode
- Data Rates up to 30 Mbps for Viterbi Mode and 90 Mbps (16-PSK) for Trellis Mode
- 3-Bit Soft Decision or 1-Bit Hard Decision Decoder Inputs for Viterbi Mode
- Viterbi Mode On-chip Channel Bit Error Rate (BER) Monitor
- Easy Implementation of Additional Code Rates
- Processor Interface Simplifies Control and Status
- Low-power CMOS Implementation
- Viterbi Mode Complies with INTELSAT IESS-308 and INTELSAT IESS-309
- Standard 84-Pin PLCC or 100-Pin VTQFP Package

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
Forward Error Correction Products Data Book, 80-24128-1 A, 8/98

http://www.qualcomm.com/ProdTech/asic
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

(4)

PERFORMANCE OF CONVOLUTION CODES

AN ERROR WILL OCCUR IN THE DECODING PROCESS WHEN THE SELECTED PATH DIFFERS FROM THE EXPECTED PATH.

LETS LOOK AT OUR RATE 1/2 K=3 CODE AGAIN. IF WE ASSUME THAT ALL PATHS ARE EQUALLY LIKELY, WE CAN LOOK AT THE CODE PERFORMANCE BY GENERATING AN ALL ZERO SEQUENCE AND THEN ADDING ERRORS

SUPPOSE M = 00000 ...

CASE 1: RECEIVED SEQUENCE : 01 00 01 00 ...
TWO ERRORS

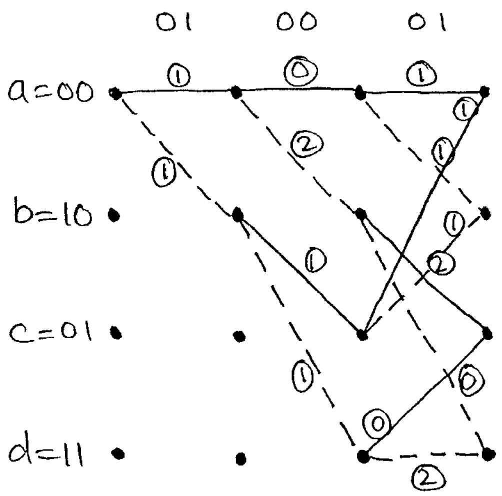
CASE 2: RECEIVED SEQUENCE : 11 000 1 00 ...
(SEE PAGES 5 AND 6) THREE ERRORS

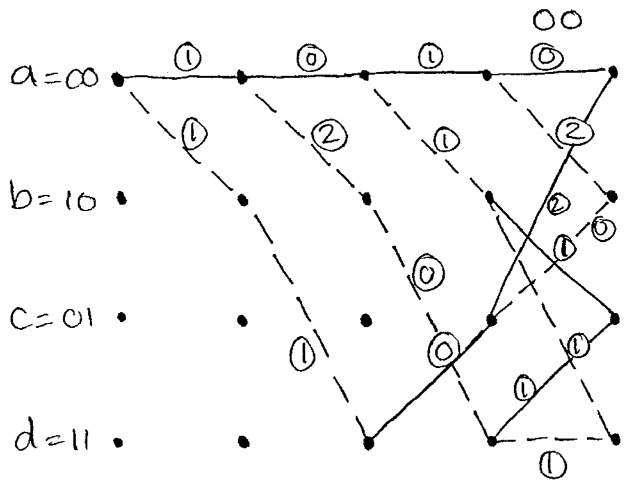
CONCLUSION : A TRIPLE ERROR IS UNCORRECTABLE BY VITERBI DECODING WHEN APPLIED TO OUR RATE 1/2 K=3 CONVOLUTION CODE

UNLESS THE TRIPLE ERROR IS SPREAD OUT OF A TIMESPAN GREATER THAN A CONSTRAINT LENGTH – IN WHICH CASE IT IS MOST LIKELY CORRECTABLE.

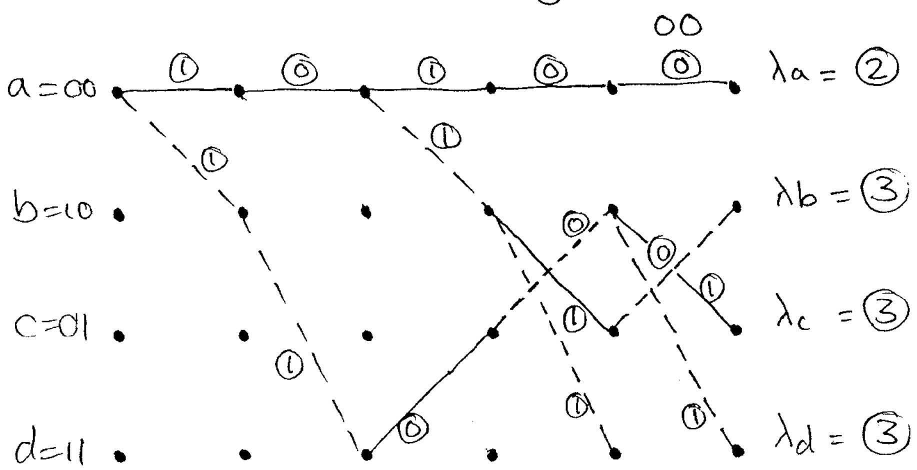
TWO ERRORS

RECEIVED SEQUENCE: 01 00 01 00 ...



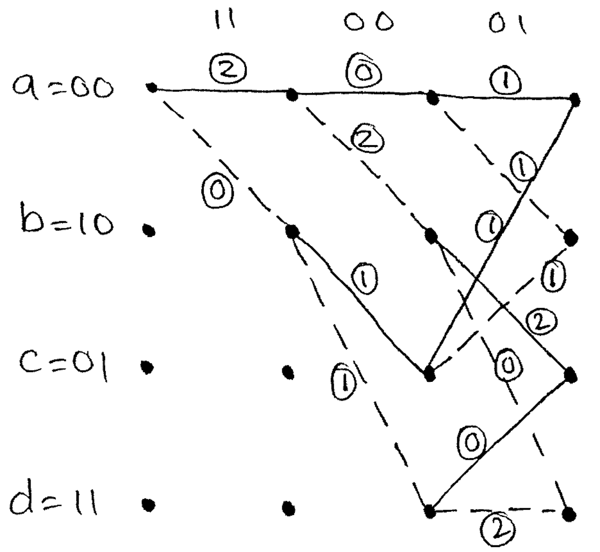


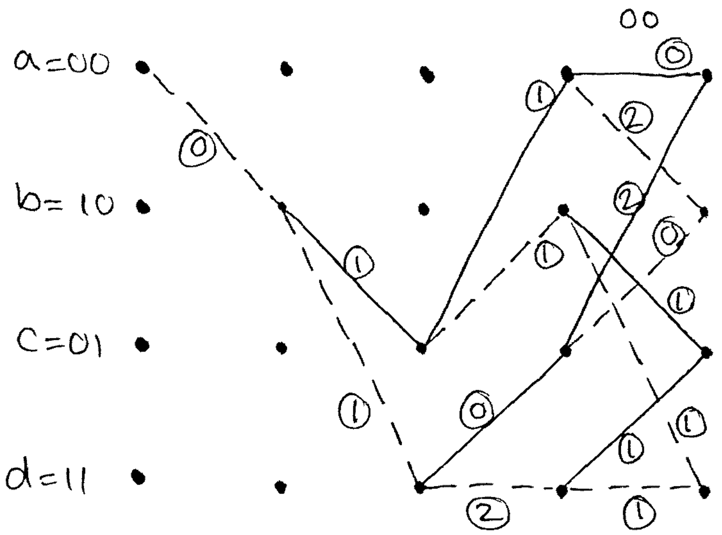
THE ALL ZERO PATH HAS THE LOWEST H.D AND ALWAYS WILL SO MESSAGE IS; 00000 ...



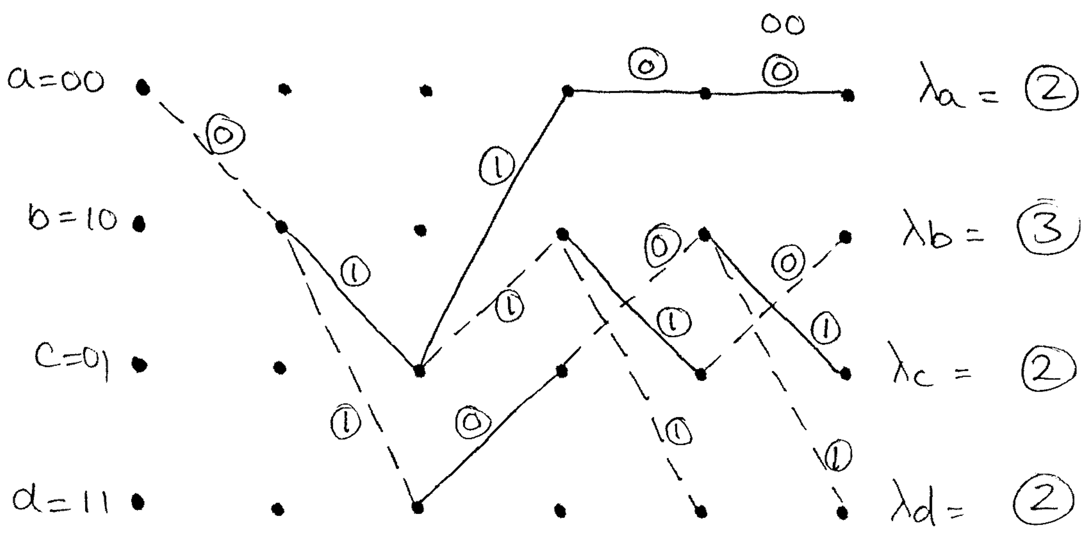
THREE ERRORS

RECEIVED SEQUENCE : 11 00 01 00





IF WE CHOOSE λa
PATH : 10000 . . .
(WE GET ONE ERROR IN THE MESSAGE)



FREE DISTANCE

RECALL THAT WE SAID EARLIER THAT AN ERROR OCCURS WHEN THE SELECTED PATH DIFFERS FROM THE CORRECT ONE.

THE MOST IMPORTANT MEASURE OF A CONVOLUTIONAL CODE'S ABILITY TO CORRECT ERRORS IS THE FREE DISTANCE d_f

FROM THE FREE DISTANCE, THE ERROR CORRECTING CAPABILITY IS GIVEN BY:

$$t = \left\lfloor \frac{d_f - 1}{2} \right\rfloor$$

(t: No CORRECTABLE ERRORS)

NOTE THE SIMILARITY WITH THE LINEAR BLOCK CODE CASE

d_f IS THE MINIMUM HAMMING DISTANCE BETWEEN ANY TWO CODEWORDS IN THE CODE, THAT BETWEEN ANY TWO PATHS IN THE TRELLIS.

WE CAN ESTIMATE THE FREE DISTANCE (SOMETIMES CALLED THE MINIMUM FREE DISTANCE) BY FINDING THE MINIMUM DISTANCE BETWEEN THE ALL-ZERO PATH (GENERATED FROM AN ALL-ZERO INPUT SEQUENCE) AND EACH OF THE OTHER CODEWORD SEQUENCE.
[SINCE THE CODE IS LINEAR WE CAN DO THIS WITHOUT LOSS OF GENERALITY]

HOW TO FIND d_f

* ASSUMING THAT THE ALL-ZEROS SEQUENCE WAS SENT, THE ONLY PATHS THAT MATTER ARE THOSE THAT START WITH STATE ØØ AND ENDS AT STATE ØØ WITHOUT RETURNING TO STATE ØØ IN BETWEEN.

* AN ERROR WILL OCCUR WHENEVER THE DISTANCE OF ANY OTHER PATH THAT MERGES WITH STATE ØØ AT TIME t_i HAS A HAMMING DISTANCE LESS THAN THAT OF THE ALL-ZEROS PATH.

* GIVEN THE ALL-ZEROS TRANSMISSION, AN ERROR OCCURS WHEN THE ALL ZEROS PATH DOES NOT SURVIVE

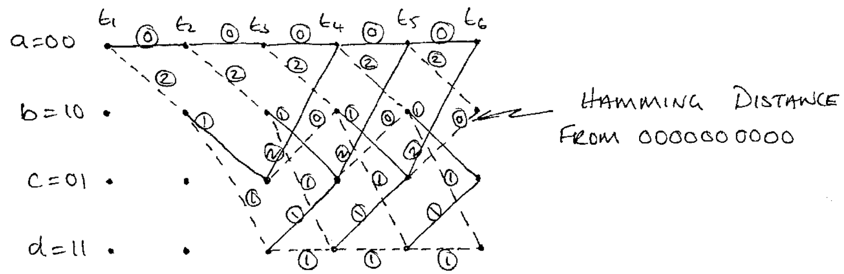
TO FIND d_f;

1) DRAW THE DECODER TRELLIS LABELLING EACH BRANCH WITH THE HAMMING DISTANCE FROM THE ALL-ZE PATH

2) EXHAUSTIVELY SEARCH ALL PATHS FROM ALL ZEROS PATH AND BACK.

3) THE MINIMUM HAMMING DISTANCE IS THE MIN FREE DISTANCE, d_f.

FOR EXAMPLE; CONSIDER OUR RATE 1/2 K=3 CODE



PATH	HAMMING DIST	# ERRORS (CORRECTABLE)
ⓐ → ⓑ → ⓒ → ⓐ	5	2
ⓐ → ⓑ → ⓓ → ⓒ → ⓐ	6	2
ⓐ → ⓑ → ⓒ → ⓑ → ⓒ → ⓐ	6	2

HENCE $d_f = 5$

CONCLUSION: THE LARGER d_f, THE BETTER THE CODE PERFORMANCE. TO INCREASE d_f WE NEED TO INCREASE K, AND OPTIMIZE THE SHIFT REGISTER CONNECTIONS

THE EXACT DESIGN OF CONVOLUTIONAL CODES IS BEYOND THE SCOPE OF THIS COURSE — IT CAN BE FOUND IN PROAKIS IF YOU'RE INTERESTED

CODING GAIN FOR A CONVOLUTIONAL CODE

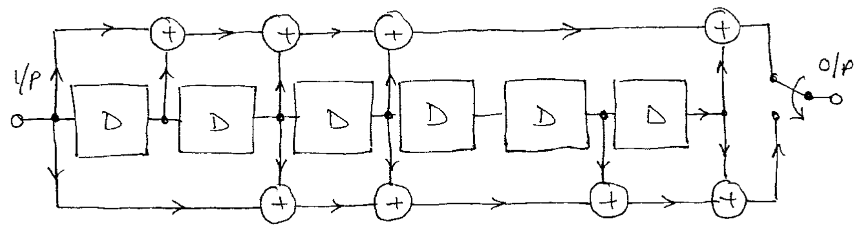
THE CODING GAIN INCREASES WITH K, HOWEVER IT CANNOT INCREASE INDEFINITELY, THE UPPER BOUND CAN BE SHOWN TO BE;

$$\text{CODING GAIN (dB)} \leq 10\log_{10}[R\, d_f]$$

WHERE R IS THE CODE RATE

R	K	d_f	MAX CODING GAIN (dB)
1/2	3	5	3.98
1/2	6	8	6.02
1/2	9	12	7.78
1/3	3	8	4.26
1/3	6	13	6.37
1/3	9	18	7.78

NASA STANDARD RATE 1/2 K=7 CODER



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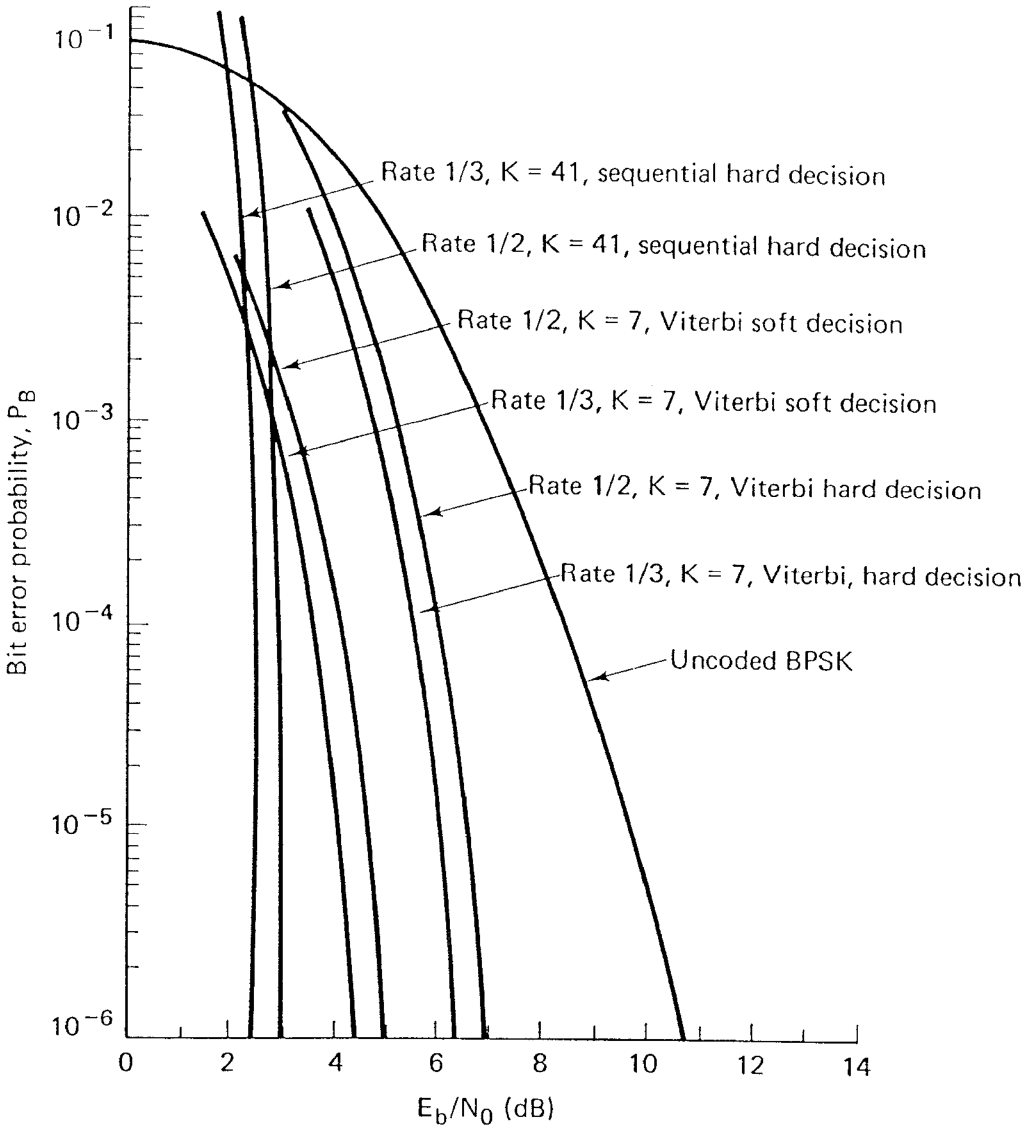

Figure 6.21 Bit error performance for various Viterbi and sequential decoding schemes using coherent BPSK over an AWGN channel. (Reprinted with permission from J. K. Omura and B. K. Levitt, "Coded Error Probability Evaluation for Antijam Communication Systems," *IEEE Trans. Commun.*, vol. COM30, no. 5, May 1982, Fig. 4, p. 900. © 1982 IEEE.)

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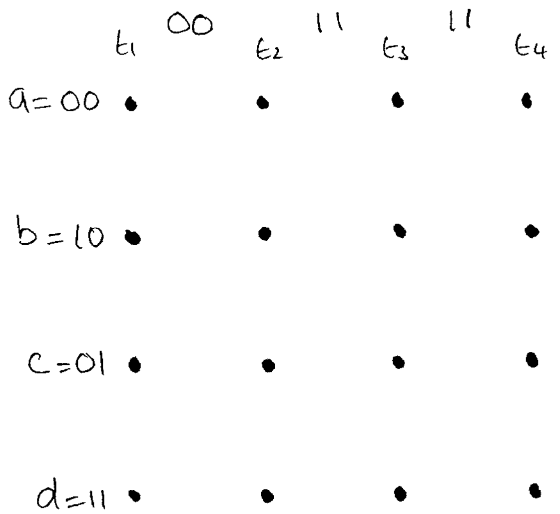

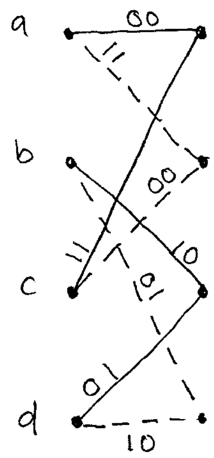

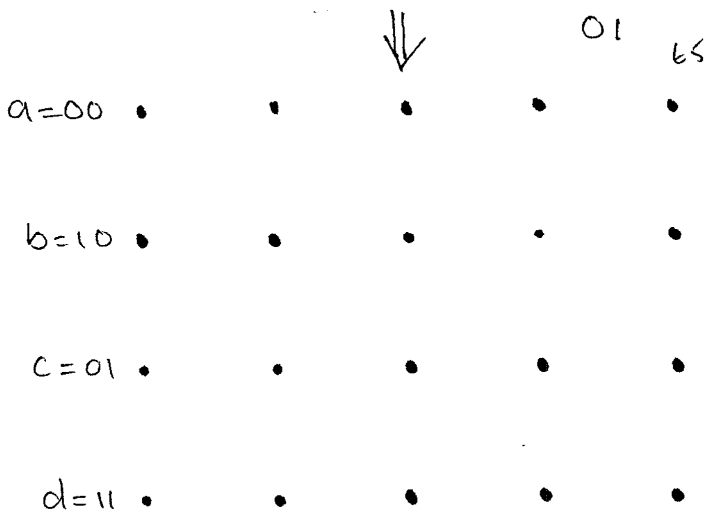

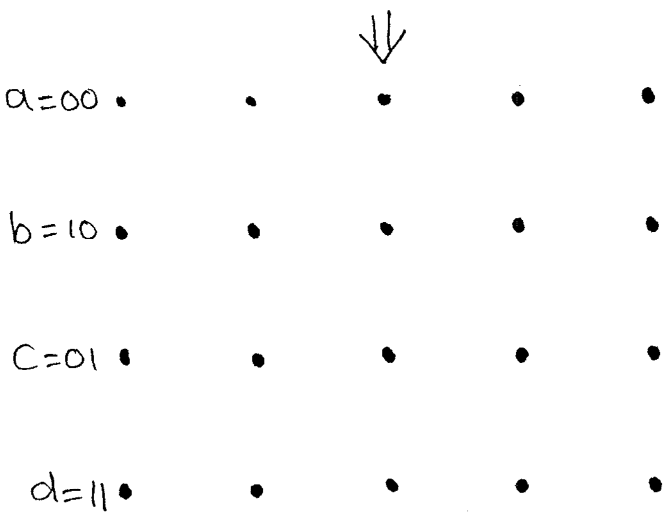

$\lambda_a =$

$\lambda_b =$

$\lambda_c =$

$\lambda_d =$

MESSAGE SEQUENCE :