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Controllable chemical vapor deposition of large area uniform nanocrystalline graphene directly on silicon dioxide

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Metal-catalyst-free chemical vapor deposition (CVD) of large area uniform nanocrystalline graphene on oxidized silicon substrates is demonstrated. The material grows slowly, allowing for thickness control down to monolayer graphene. The as-grown thin films are continuous with no observable pinholes, and are smooth and uniform across whole wafers, as inspected by optical-, scanning electron-, and atomic force microscopy. The sp^2 hybridized carbon structure is confirmed by Raman spectroscopy. Room temperature electrical measurements show ohmic behavior (sheet resistance similar to exfoliated graphene) and up to 13% of electric-field effect. The Hall mobility is $\sim$40 cm^2/Vs, which is an order of magnitude higher than previously reported values for nanocrystalline graphene. Transmission electron microscopy, Raman spectroscopy, and transport measurements indicate a graphene crystalline domain size $\sim$10 nm. The absence of transfer to another substrate allows avoidance of wrinkles, holes, and etching residues which are usually detrimental to device performance. This work provides a broader perspective of graphene CVD and shows a viable route toward applications involving transparent electrodes. © *2012 American Institute of Physics*. [doi:10.1063/1.3686135]

I. INTRODUCTION

Graphene, a single-atomic plane of sp^2 hybridized carbon atoms, is a remarkable material with extraordinary electrical and optical properties by virtue of its unique band structure. The experimentally measured conductance indicates high and approximately equal mobilities for holes and electrons. Graphene is transparent; it absorbs $\pi\alpha \approx 2.3\%$ of white light, where α is the fine-structure constant.[1] It is expected that graphene will play a crucial role in future nanoelectronics[2] and optoelectronics.[3] Traditionally, graphene is produced by mechanical exfoliation of graphite,[4] a process intrinsically limited to the formation of small flakes (typically a few μm in size) unsuitable for most industrial applications. To date, techniques which are capable of producing large area graphene include epitaxial growth and chemical vapor deposition (CVD). The epitaxial technique where SiC substrates are heated to high temperatures to sublimate the Si, leaving the C to form one or more graphene layers,[5] is costly due to the quality and size requirements on the substrates. On the other hand, the CVD technique is cost-efficient and scalable. It is compatible with existing semiconductor technologies and is far more realistic for use in industrial processes.[6] In the CVD of graphene, metals, such as Cu (Ref. 7) or Ni (Ref. 8) are commonly used as catalysts. However, since they are electrically conducting, transfer of the synthesized graphene onto insulators is required for most applications. Wrinkles, holes, and metal etching residues are inevitable during such transfers and often result in decreased device performance or even failure. For practical applications, a reliable large scale deposition of graphene directly on insulators is highly desirable. Recent advances in a metal-free growth of graphene include CVD (or molecular beam epitaxy (MBE)) on sapphire,[9,10] ZnS,[11] BN,[12] GaN,[13] Si_3N_4,[14] MgO,[15] and HfO_2,[14] etc. Graphene produced without metal catalysts is nanocrystalline, and therefore the carrier mobility is low (typically $\sim$1 cm^2/V s),[9] and thus unsuitable for transistors. Nevertheless, it is very promising for other important applications, such as transparent electrodes[16] and sensors.

In particular, the direct synthesis of graphene on standard dielectric SiO_2 is one of the important goals which the semiconductor industry is pursuing.[17] This, however, has been widely found to be extremely difficult. The process is usually reported as irreproducible yielding discontinuous graphene with unknown electrical properties.[17–20] On the other hand, the formation of graphitic carbon on SiO_2 has been known for several decades,[21,22] but has thus far been overlooked with regard to graphene synthesis. In this paper, we have explored the potential of this effect and demonstrated that large area uniform nanocrystalline graphene can be grown directly on oxidized Si substrates by CVD without using any metal catalysts. The growth conditions are very different from those of metal-catalyzed CVD of graphene. The thickness of graphene is controllable by changing the deposition time and/or

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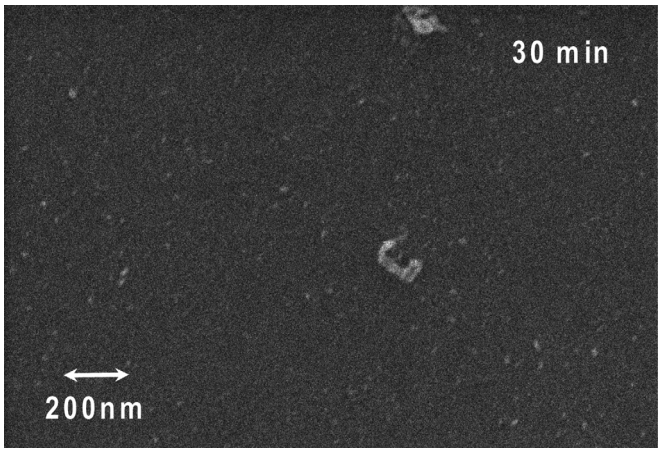

FIG. 1. SEM micrograph of the nanocrystalline graphene grown for 30 min directly on 300 nm SiO_2.

precursor partial pressure. The thin films are wrinkle-free, have no observable pinholes, and are uniform across entire wafers, as inspected by optical, scanning electron- and atomic force microscopy (SEM and AFM). Raman spectra confirm the sp^2 hybridized carbon structure. Room temperature electrical characterization reveals ohmic behavior and electric-field effect. Transmission electron microscopy (TEM), Raman spectroscopy, and transport measurements all imply a crystalline domain size ~10 nm. The carrier mobility is ~40 cm^2/Vs, which is an order of magnitude higher than previously reported for graphene grown on sapphire.[9] The transfer-free fabrication reported here demonstrates a significant step toward large scale graphene synthesis on dielectric materials and its exploitation in future applications involving transparent electrodes.

II. EXPERIMENTS

The CVD is performed in a home-built atmospheric-pressure hot-wall quartz tube furnace. CH_4 is used as a carbon precursor gas, mixed with auxiliary reduction- (H_2) and carrier (Ar) gases. 300-nm-thick SiO_2 thin films are grown by a standard wet oxidation of Si wafers (using oxyhydrogen at 1050 °C). These substrates are heated to 1000 °C (at a rate of ~30 °C/min) under H_2 (50 sccm) and Ar (1000 sccm) atmosphere and kept at 1000 °C for 3 min. Then, 300 sccm CH_4 is introduced to initiate the formation of graphene. The typical growth time is 30–60 min. After the deposition, the CH_4 flow is stopped, leaving other gases to flow for further 3 min to remove residual reaction gases before allowing the chamber to naturally cool to room temperature (~20 °C/min) in the same $H_2 + Ar$ atmosphere. The nanocrystalline graphene can also be deposited directly on SiO_2 by using other hydrocarbon precursors, such as C_2H_2, showing the generality of the process (for details, see Supplementary Materials[23]).

III. RESULTS AND DISCUSSION

The graphene thin films directly grown on SiO_2 are very uniform over large areas with no visible wrinkles, which can be confirmed by SEM (see Fig. 1). However, there are some particles on the surface, most likely due to the co-deposition of nanographite during growth. Considering that the deposition rate is low, the thickness of the graphene on SiO_2 can easily be controlled while keeping high uniformity across large substrates simply by tuning the growth time. For TEM analysis, the samples are first coated with polymer (e.g., PMMA) support and subsequently immersed in diluted HF acid to separate the graphene from SiO_2/Si substrates. After rinsing, the thin films are transferred to Cu TEM grids with a holey carbon network followed by removal of the polymer by acetone. Figure 2 shows high-resolution TEM images of the graphene grown for 30 min. The graphene is continuous and uniform. Nanographite is occasionally found (indicated by arrows in Fig. 2 (b)), where the layered structure of the particles is visible. In Fig. 2(a), at the rippled/folded free-standing edge of the films, layer-by-layer structure is observed. Figure 2(c) shows a typical convergent beam electron diffraction pattern obtained from almost every place in the sample, which is a clear signature of the hexagonal lattice structure from single-layer graphene. However, we notice that if the electron beam is moved over a distance of a few nm or if the beam spot is bigger than ~10 nm, diffraction patterns like in Fig. 2(d) are observed. The mixed monolayer graphene signals imply that the beam is either at domain boundaries or covers several domains. Figure 2 provides a direct evidence of the CVD monolayer graphene and indicates a nanocrystalline grain size of ~10 nm.

Optical micrographs of the as-grown graphene are shown in Figs. 3(a) and 3(b), corresponding to the growth time of 30 and 60 min, respectively. The left section of each image shows a transferred graphene grown by standard Cu-catalyzed CVD for comparison.[24] As is generally

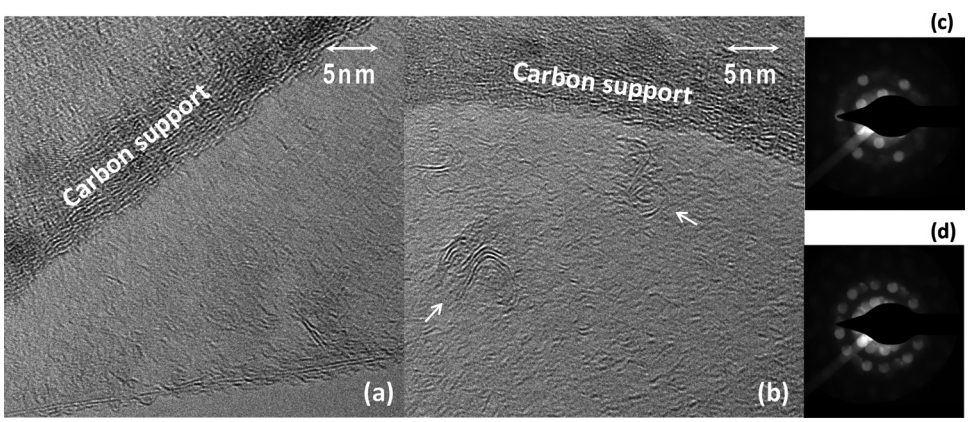

FIG. 2. (a) and (b) Plan-view TEM images of the graphene directly grown on SiO_2/Si for 30 min. At the bottom of (a), a layered structure at the free-standing edge is seen, as graphene tends to roll up at free edges during transfer to TEM grids. In (b), the arrows indicate co-deposited nanographite. (c) A typical convergent beam electron diffraction pattern showing unique features from monolayer graphene. (d) A diffraction pattern showing signals from more than one domain, in correspondence with the nanocrystalline structure.

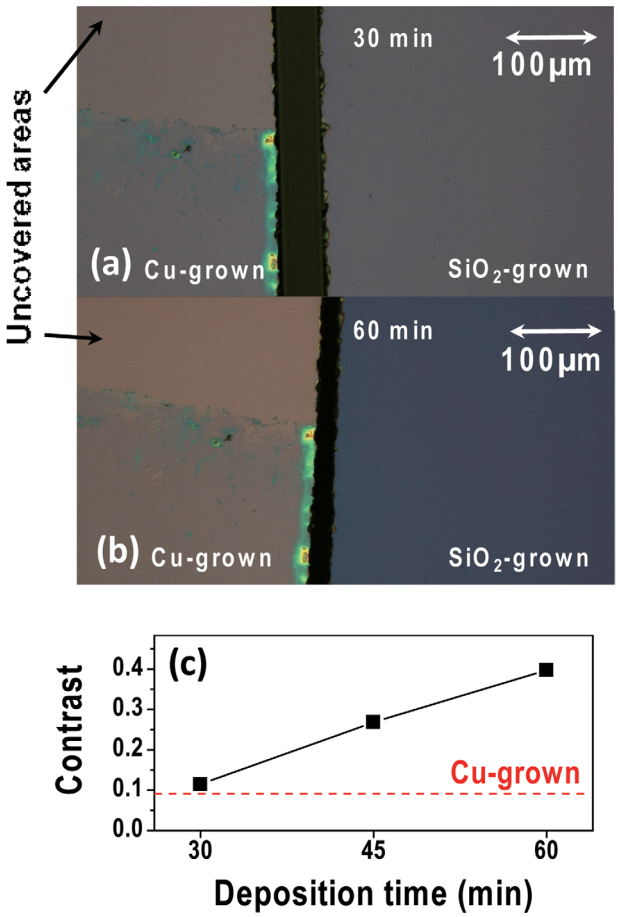

FIG. 3. (Color online) (a) and (b) Optical images of the graphene thin films deposited directly on SiO_2 (300 nm) from CH_4 precursor during 30 and 60 min, respectively. In each micrograph, the left section is a transferred Cu-grown graphene for comparison of optical contrast. (c) Average contrast of the graphene images vs deposition time. The dashed line indicates the contrast of the Cu-catalyzed graphene for comparison.

acknowledged,[6,7,16,18,19,24–26] and also confirmed by our Raman measurements (see Fig. 4(a)), the graphene grown on Cu is primarily monolayer. In Fig. 3(a), the two samples have almost equal color and contrast. Thus, it is reasonable to conclude that the graphene grown on SiO_2 is composed of primarily monolayer crystallites in this figure, in agreement with the TEM observation. The inset of Fig. 5(a) shows the AFM-height profile across a step in the thin film, revealing a step height ~2 nm. Typically, monolayer graphene fabricated by mechanical exfoliation has an AFM-measured thickness of ~0.8 nm on SiO_2, whereas after lithographic processing this thickness often increases to ~1.5–2 nm,[27,28] also in agreement with our data. However, according to Figs. 1 and 2, the coexistence of a number of few-layer graphene flakes (or nanographite) indicates that Fig. 3 represents a macroscopically average effect of these flakes as well as the grain boundaries. Longer growth time leads to thicker graphene. The contrast of the samples grown during 30, 45 (not shown), and 60 min are compared with the Cu-grown graphene in Fig. 3(c). Here, the contrast is defined as $(D_{sub}-D_{gr})/D_{sub}$, where D_{gr} and D_{sub} are the average brightness of the graphene and the substrate (uncovered areas in Fig. 3(a)), respectively. Not unexpectedly, increasing the amount of CH_4 in the growth chamber for a fixed deposition time also results in a thicker graphene. In the extreme case of 30 min CVD at 1000 sccm CH_4 and 50 sccm H_2 (as compared to our regular recipe of 300 sccm CH_4, 50 sccm H_2, and 1000 sccm Ar in the Experiments) we obtain thick nanocrystalline graphite films (not shown). Note that the as-synthesized films retain a metallic luster even for hundreds of layers.[14,29] Figure 3 is obtained by an optical microscope and the data are thus not quantitatively accurate enough to be evidence of monolayer graphene. However, since the thickness variation in SiO_2 on different chips is in the order of only ~1 nm, Fig. 3 is sufficient for a convenient estimation of thickness. We have performed variable angle spectroscopic ellipsometry (VASE) to obtain more rigorous optical information.[29] The nanocrystalline graphene grown for 30 min shows results which are qualitatively similar to what has been reported recently on exfoliated and Cu-grown monolayer graphene.[30,31] Nanocrystalline graphene deposited using a similar recipe on single crystal SiO_2 (quartz) also shows properties similar to standard graphene, as measured by transmission spectroscopy,[29] respectively.

Graphitization is a complex physicochemical phenomenon and the detailed mechanism is not yet understood. Here, we propose two possible scenarios of the CVD of our nanocrystalline graphene. The first mechanism is a self-assembly of nanographene flakes resulting from pyrolysis of CH_4.[14,29] At 1000 °C, most of the CH_4 molecules decompose. The released carbon atoms readily arrange themselves in aromatic rings and planar sp^2 hybridized graphitic layers forming nanographene crystallites up to ~10 nm in size. Under usual conditions, the nanographene chaotically aggregates into bigger porous lumps with rough surfaces, such as carbon black.[32,33] In our case, a hot flat substrate forces the nanographene to orient itself parallel to the substrate thereby initiating the growth of textured thin films. The high substrate temperature and presence of H_2 favor larger crystallites at the surface as they are thermodynamically more stable, while the smaller ones (thin-film nuclei) are easier to decompose or react with H_2. However, the small crystallites may survive at lower temperature, thereby breaking the self-assembly process that results in the ordered structure of the thin film. Indeed, at the lower-temperature zones of the CVD reactor tube we only observe porous deposits reminiscent of soot. We anticipate that this mechanism would permit growing continuous nanocrystalline graphene on virtually any dielectric substrate that withstands ~1000 °C.[14,29] The second mechanism of the CVD of graphene on SiO_2 might be of catalytic nature. The catalytic graphitization by SiO_2 powder was observed previously.[21] It is explained by the formation and decomposition of surface carbide intermediates[21] and is presumably related to the fact that Si can catalyze graphitization.[34] In our experiments on bare Si, nanocrystalline graphene can indeed be easily obtained at merely 700 °C (see Supplementary Materials[23]).

The Raman spectra of graphene grown on Cu and nanocrystalline graphene grown on SiO_2 are shown in Fig. 4. The G and 2D bands located at ~1591 cm^{-1} and ~2683 cm^{-1}, respectively, are clearly seen for all samples. These two peaks are characteristic spectral features of graphitic sp^2 hybridized materials. The well-defined peaks differentiate the as-produced nanocrystalline graphene from amorphous

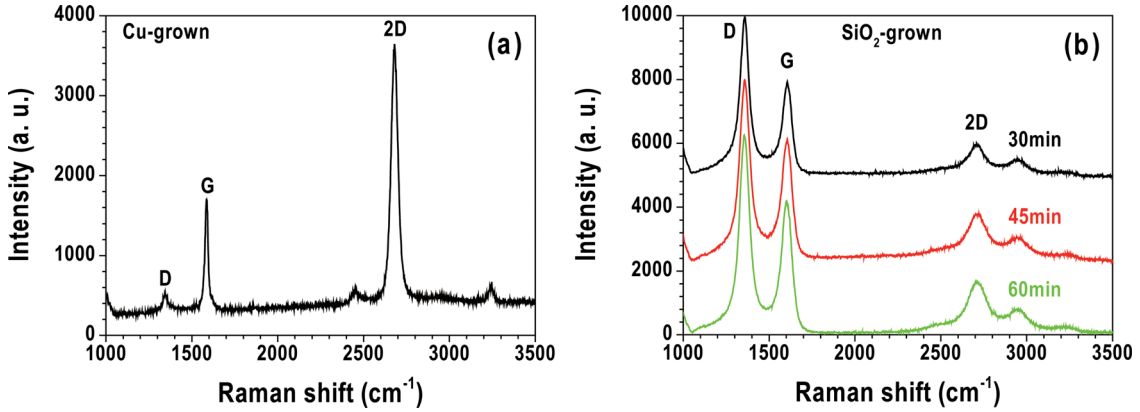

FIG. 4. (Color online) Raman spectra (514 nm, × 100 objective, 0.5 mW) of graphene grown by CVD. (a) Typical Raman signatures of Cu-grown graphene (transferred to 300 nm SiO_2/Si substrate). (b) Raman spectra of nanocrystalline graphene deposited directly on 300 nm SiO_2/Si for 30, 45, and 60 min. For all the samples, the G and 2 D spectral peaks are clearly observed. Curves have been shifted along the ordinate for clarity.

carbon (*a*-C).[35] Typically, the Raman spectra of *a*-C have very broad G and D bands merged together, and the 2D band is absent, as summarized by two groups.[36,37] In fact, atomically thin *a*-C films have only recently been made by bombarding graphene with an electron beam.[38] In Fig. 4(a), the 2D-to-G peak-height ratio is ~2 and the full width at half maximum (FWHM) of the symmetric 2D peak is ~37 cm^{-1}. This implies that the Cu-grown graphene is indeed a high-quality monolayer.[7] In comparison, the SiO_2-grown graphene has higher D peaks at about 1350 cm^{-1}, as seen in Fig. 4(b). The G + D band (high-order Raman signals) at ~2941 cm^{-1} (Refs. 39 and 40) is also detected. Raman D band is a fingerprint of disorder in the sp^2 network of carbon materials. The ~10 μm laser spot in our Raman measurements covers numerous graphene domains with random in-plane orientations resulting in a strong D peak. By analyzing the I_D/I_G intensity ratio, disorder in the graphene monolayer can be (roughly) quantified. Using the model proposed by Lucchese *et al.*,[35,41] the average distance between defects is estimated to be 7–8 nm, i.e., consistent with the graphene grain size of ~10 nm determined by TEM and transport measurements (see below).

Hall bar structures are patterned on the as-synthesized thin films by conventional photolithography using S1813 photoresist. As electrode materials, 5 nm Cr and 45 nm Au are deposited by evaporation. A typical optical micrograph of the completed device is shown in the inset of Fig. 5(b). All electrical measurements shown in this figure are performed at room temperature in air without sample annealing. Voltage V is applied between the two horizontal contacts (1, 4) while recording the current I. The other electrodes permit four-terminal measurements over 4×4 μm^2 of the active area of the device. The transport properties are similar for all devices on the same chip, highlighting the reproducibility of the synthesis process and the uniformity of the thin films. Figure 5(a) plots the *I-V* curves of devices made from samples grown during various times. Linear (ohmic) behavior is observed for all samples, including the contact resistances to metal electrodes. The sheet resistances R_s obtained in the four-probe measurements are 13.3, 6.8, and 5.4 kΩ/□ for the samples grown during 30, 45, and 60 min, respectively, i.e., R_s decreases as the film thickness increases. The value for the 30-min-grown sample is larger than but still comparable to that of the Cu-produced monolayer graphene.[26] Figure 5(b) depicts the field effect in the graphene. Back-gate voltage V_g

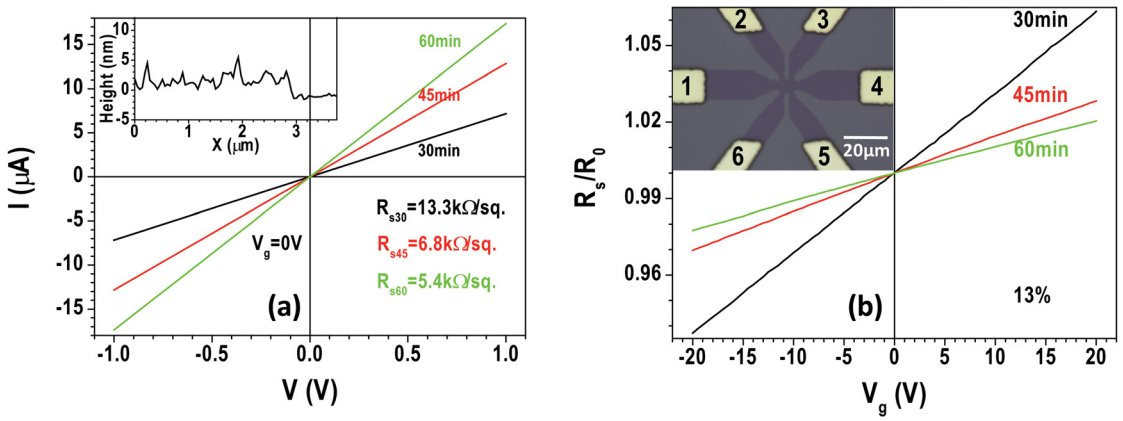

FIG. 5. (Color online) (a) The two-probe *I-V* curves of devices made on samples with various deposition time. The sheet resistance R_s is calculated from the four-probe configuration. Inset: an AFM line scan on a device made from the 30-min-grown sample, showing a step height of ~2 nm. (b) The field effect in the nanocrystalline graphene. The sheet resistances (normalized to R_s at zero V_g) are plotted against the gate voltage. Inset: the optical micrograph of the device layout. The active area is 4 μm × 4 μm.

is applied to the conducting underlying Si substrate, which is capacitively coupled to the thin films via 300-nm-thick SiO_2. For the 30-min-grown sample, R_s varies by approximately 13% under ±20 V gate voltages, while a weaker field effect is seen in samples grown for longer times. The Dirac point is not observed at this V_g range, possibly due to the charge doping effects from the photoresist.[42] Recently, it is found that high-temperature annealing can reduce the distance between exfoliated graphene flakes and SiO_2 substrates, thereby increasing the coupling between them, and leading to heavy hole doping and severe mobility degradation.[28] This can account for our reduced gating performance, since the graphene is synthesized in a long-time high-temperature process.

Hall measurements have been carried out on the device shown in the inset of Fig. 5(b). At both room- and low temperatures, the Hall mobility is ~40 cm^2/Vs, an order of magnitude improvement compared with the previously reported best result for nanocrystalline graphene thin films.[9] The value is also in good agreement with the mobility extracted from the gate measurements shown in Fig. 5(b).[43,44] Based on the Hall-effect and magnetoresistance studies, independent estimation of the graphene grain size can be obtained. The results are shown in Fig. 6 where the magnetoconductance (MC) $\Delta\sigma(B) = R_s^{-1}(B) - R_s^{-1}(0)$ is presented for several temperatures from 3.8 to 290 K. In these experiments, R_s and the Hall resistance R_H have been determined by taking the symmetric and antisymmetric components of the voltage V_{25} across contacts 2 and 5 while applying the current $I = 1$–10 μA between contacts 1 and 4: $R_s = [V_{25}(B) + V_{25}(-B)]/2I$ and $R_H = [V_{25}(B) - V_{25}(-B)]/2I$

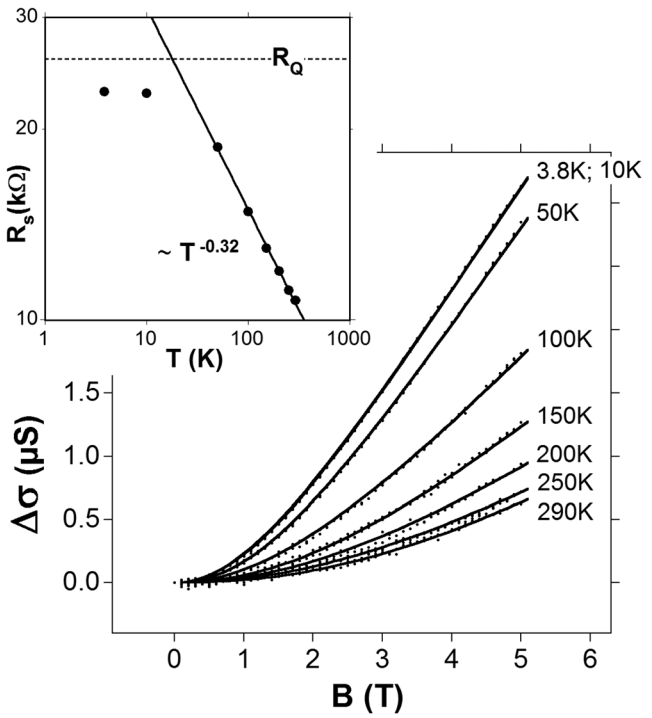

FIG. 6. The magnetoconductance $\Delta\sigma(B)$ at different temperatures indicated. The inset shows the temperature dependence of the zero-field resistance R_s. The dashed line indicates the quantum resistance $R_Q = e^2/h \approx 25.8$ kΩ. The solid line is the power-law fitting for $T \geq 50$ K.

(see Fig. 5). The MC is positive (magnetoresistance negative) and non-zero even at room temperature. The negative magnetoresistance is characteristic for many disordered materials,[45] and in particular, for carbon-based systems.[46–49] It is usually explained by the weak localization of carriers with some peculiarities which are characteristic for graphene (see Refs. 46, 50, and references therein). The electron mean free path l in our thin films is clearly small, because e.g., R_s is close to the quantum resistance R_Q at low temperature meaning that $k_F l \lesssim 1$, where k_F is the Fermi wave vector. Thus, the electron localization is rather strong and the conductivity can be described by the variable-range hopping model[51] with $\ln(\sigma(T)) \sim T^{-1/3}$ in the two-dimensional case. This is consistent with $R_s(T)$ shown in the inset of Fig. 6. It has been argued that the weak-localization analysis can be used even in the case $k_F l \lesssim 1$.[47] Indeed, our $\Delta\sigma(B)$ data can be fitted very well by the weak-localization equation, $\Delta\sigma(B) = e^2[3F(4eL_1^2B/\hbar) - F(4eL_0^2B/\hbar)]/(2\pi h)$, where $F(x) = \psi(0.5 + 1/x) + \ln(x)$ and $\psi(x)$ is the digamma function, with two cumulative fitting parameters, L_0 and L_1, which are the characteristic singlet and triplet dephasing lengths, also including spin effects[47,50] (see Fig. 6). Both L_0 and L_1 are about 10-11 nm at low temperature decreasing to 6–7 nm at room temperature. However, the accuracy of experimental $\sigma(B)$ is not sufficient to firmly extract the spin-related components of L_0 and L_1.

IV. SUMMARY

We have demonstrated that atomically thin nanocrystalline carbon films can be fabricated on standard SiO_2 dielectric by direct CVD without metallic catalysts. The uniform morphology of the graphene is observed by optical microscopes as well as SEM, AFM, and TEM. The sp^2 carbon network is confirmed by Raman measurements. The growth mechanisms of the thin films are briefly discussed. The as-deposited graphene shows ohmic behavior and electric-field effect at room temperature. The disorder-induced negative magnetoresistance is observed. TEM, Raman, and transport analysis all agree with the graphene nanocrystallites in the size range of ~10 nm. We anticipate that our results will stimulate further investigation on the use of oxides in the CVD of graphene. The transfer-free process detailed here favors the industrialization of graphene technology and hints at a promising future in a wide variety of applications, such as transparent electrodes and other applications relying on cheap and chemically stable ultrathin conducting coatings.

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