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All-Chemical Vapor Deposited Graphene/Silicon Nitride TFTs

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All-chemical vapor deposited silicon nitride / monolayer graphene TFTs have been fabricated. Polychromatic Raman spectroscopy shows high quality monolayer graphene channels with uniform coverage and significant interfacial doping at the source-drain contacts. Nominal mobilities of approximately 1900 $cm^2V^{-1}s^{-1}$ have been measured opening up a potentially useful platform for analogue and RFR-based applications fabricated through all-chemical vapor deposition processes.

Graphene is a one atomic thick layer of carbon atoms, where their sp^2 bonds are arranged in a honeycomb crystal lattice. It is being touted as the new "miracle material" for electronics and photonics in the 21st Century. This is because of its unique properties such as the very high carrier mobility at room temperature, large free mean path for ballistic transport, high Young's modulus and near zero-gap semiconductor (semi-metal). These make it potentially unique for nano-electronics, biosensors and information and computer technologies. Early graphene transistor configurations consisted of back-gated metal-oxide-semiconductor field effect transistors. Alternative top-gate configurations include the use of channels formed from high-quality natural and Kish exfoliated graphene, CVD grown and polymer transferred graphene and epitaxial deposited samples. SiO_2, Al_2O_3, and HfO_2 have been investigated as viable dielectrics in zero band gap devices. Graphene transistors exhibit linear transfer characteristics without saturation or weakly saturate followed by a secondary linear regime[1]. Due to the low on/off current ratio, graphene-based devices are unsuitable for logic applications through various routes to bandgap opening have been proposed, such as the use of sub-5 nm-wide nanoribbons [2], mechanically strained free-standing channels, and biased bilayers[3].

The dielectric is known to affect the charge carrier type in graphene devices[4]. SiN_x has been successfully used as a dielectric for TFTs within flat-panel displays for many years, yielding a mature and widely accepted technology, which is, for example, routinely used in *a*-Si backplanes for organic light-emitting diode displays[5]. In this work, we show TFTs based on monolayer graphene as the active channel material with SiN_x as the insulator where both materials have been produced using chemical vapor deposition (CVD) processes. Though low on/off ratios mitigate against their use in logic circuits they are well suited for analog RF applications, in body area networks and some flat panel applications.

Bottom gated graphene TFTs were produced on 300 nm thick SiN dielectric layers deposited by PECVD onto degenerately doped silicon substrates. SiN_x was deposited at 150°C using radio frequency plasma enhanced chemical vapor deposition (RF-PECVD)

at 13.56 MHz. Source and drain contacts, 500 nm wide and of various channel lengths (5-50 nm) were defined by either standard photolithography or electron beam lithography followed by the evaporation of Ti/Au contacts of thickness 1nm/40nm, as indicated in figure 1.

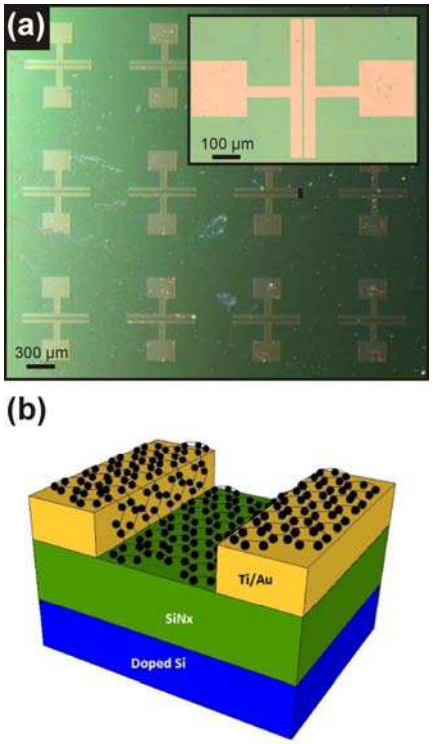

Fig. 1 (a) An optical micrograph of several as-fabricated TFTs. Channel lengths vary from 5 µm to 50 µm (Scale bar: 300 µm). The inset shows a detailed view of a single device with a 500 µm wide channel. (Scale bar: 100 µm). **(b)** Schematic showing the device stack and monolayer graphene channel.

Graphene was grown by thermal CVD in a commercially available cold walled CVD reactor (Aixtron Ltd) using Cu foils (99.99%) as the catalyst layer. The as-grown graphene was transferred onto silicon nitride samples using spin coated polymethylmethacrylate and Cu under etching of 25% wt. ferric chloride, as reported elsewhere e.g. [6].

In-situ polychromatic Raman spectroscopy at 457 nm, 532 nm and 633nm, directly on the Cu catalyst substrates, prior to the graphene transfer, as well as following the transfer process, showed the quality of the as-grown material with signatures consistent with those of extremely high-quality primarily monolayer kish-exfoliated graphene (Fig. 2). Single Lorentzians were well-fitted to the 2D peak (2690 cm^{-1}), strongly suggesting the presence of monolayer graphene (Fig. 2a), with a narrow mean full-width half-maximum of 36.85 (±1.22) cm^{-1}.

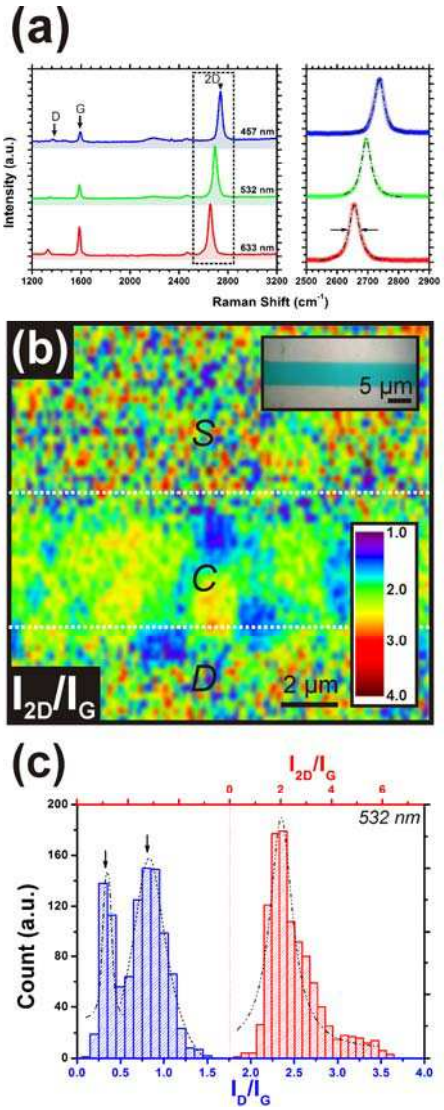

Fig. 2. (a) Raman spectra of the pristine CVD grown monolayer graphene channel performed at 457 nm, 532 nm, and 633 nm (incident power < 3 mW) evidencing signatures characteristic of extremely high-quality monolayer graphene. **(b)** 532 nm I_{2D}/I_G map of a typical graphene channel (Scale bar: 2μm). **(c)** Histogram, and Guass fits, of I_D/I_G (blue) and I_{2D}/I_G (red) for a transferred sample.

The transferred material was highly crystalline with a low defect density, evidenced by an I_D/I_G ratio of 0.07 (±0.06), though this reduced to 0.34 (±0.12) once transferred due to substrate interactions. The I_{2D}/I_G = 4.63/2.36 (±1.18/2.02) (pristine/transferred) also suggests a monolayer material and spatially resolved 532 nm Raman spectroscopy indicates minimal doping induced in the monolayer graphene channel (in contact with the SiNx substrate) whilst significant doping is noted at the Ti/Au contacts though a >99 % monolayer channel is evident. Bimodal peaks are observed in the I_D/I_G statistics due to the doping effects at the metallic interfaces.

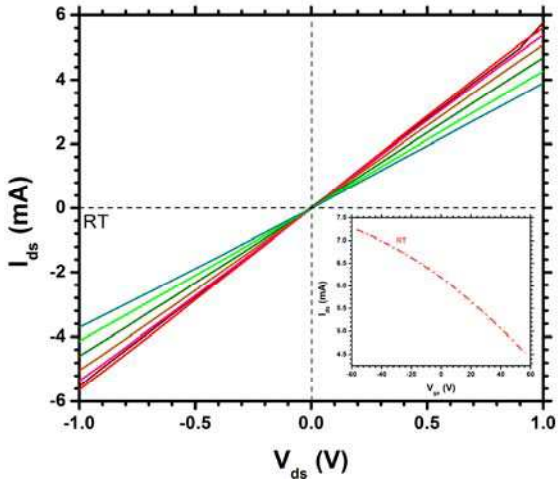

Fig. 3. D.C drain-source voltage (V_{ds}) as a function of drain current (I_{ds}) at different gate voltage (-60V (red) <V_G<60V (blue) *Inset:* Typical I_{ds} against V_{gs} at room temperature (RT). W = 500 μm and L = 25 μm.

The transfer characteristics (Fig. 3) show nominally *p*-type operation with a hole mobility of 1900 $cm^2V^{-1}s^{-1}$, as discussed below. All graphene TFTs were measured at room temperature. Figure 3 shows the typical response of the I_{ds} to V_{ds} for the as-prepared graphene TFT samples. With the gate voltage ramped from -60 V to 60 V (as shown in inset), the I_{ds} decreased from 7.3 mA to 4.5 mA, indicating that as-prepared graphene was heavily *p*-typed. This may be caused by the absorption of water molecules from air or/and PMMA residue from the transfer process[7]. Thus, the Dirac point is outside the range (V_G = 260 V) of the gate voltages that were studied. As shown above the I_{ds} vs V_{ds} characteristics of graphene TFTs show a linear behavior without any saturation.

The Dirac bias can be derived from the concept of minimum conductivity[8], as;

$$\sigma = \sigma(V_{gs} = 0) - \frac{d\sigma}{dV_{gs}} \cdot V_G, \quad where \quad \sigma = \frac{I_{ds} L}{V_{ds} W t}$$

$$\sigma = I_{ds} k, \quad where \quad k = \frac{L}{V_{ds} W t}$$

$$I_{ds} = I_{ds}(V_{gs} = 0) - \frac{dI_{ds}}{dV_{gs}} \cdot V_G$$

where I_{ds} is the drain-source current, L = 25 μm, is the gate length, W = 500 μm, is the gate width, t = 0.34 nm, is the graphene thickness, V_{ds} = 1 V, bias voltage. The conductivity is linearly proportional to I_{ds}.

For a minimum,

$$0 = I_{ds}(V_{gs} = 0) - \frac{dI_{ds}}{dV_{gs}} \cdot V_G$$

$$\Rightarrow V_G = I_{ds}(V_{gs} = 0) \frac{dV_{gs}}{dI_{ds}} \quad (1)$$

And the field-effect mobility is;

$$\mu_{FE} = \frac{dI_{ds}}{dV_{gs}} \cdot \frac{1}{W/L \cdot C_{ox} \cdot V_{ds}} \quad (2)$$

where C_{ox} is the gate capacitance. Given that [8]

$$p = \frac{C_{ox}}{e} V_G \Rightarrow C_{ox} = \frac{pe}{V_G} \quad (3)$$

Substituting (1) into (3), and (3) into (2), the equation for mobility becomes ;

$$\mu_{FE} = \frac{I_{ds}(V_{gs} = 0)}{W/L \cdot p \cdot e \cdot V_{ds}}$$

Using the above equation, we find a mobility of approximately 1900 $cm^2V^{-1}s^{-1}$, a value which is consistent with intrinsic graphene. We have not considered possible contact resistance effects; the mobility can be larger in longer channel TFTs.

In summary, we have fabricated and characterized bottom-gated monolayer thermal CVD graphene TFTs on SiN_x gate dielectric deposited by PE-CVD. Our data, both modeled and empirical suggests nominally *p*-type transfer characteristics, giving extracted mobilities of approximately 1900 $cm^2V^{-1}s^{-1}$ at room temperature. These preliminary results offer a promise for industry compatible high-speed TFTs fabricated *via* all-chemical vapor deposition processes.

References

1. I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors.," *Nat. Nanotech.*, **3** (11), pp. 65, (2008).

2. Z. Chen, Y. Lin, M. Rooks, and P. Avouris, "Graphene nano-ribbon electronics," *Phys. E: Low-dim. Sys. Nanostruc.*, **40** (2), pp. 228-232 (2007).

3. P. Gava, M. Lazzeri, a. Saitta, and F. Mauri, "Ab initio study of gap opening and screening effects in gated bilayer graphene," *Phys. Rev. B*, **79** (16), pp. 1-13, (2009).

4. A. Konar, T. Fang, and D. Jena, "Effect of high-κ gate dielectrics on charge transport in graphene-based field effect transistors," *Phys. Rev. B*, **82** (11), pp. 1-7, (2010).

5. F. M. Li, A. Nathan, Y. Wu, and B. S. Ong, "Organic thin-film transistor integration using silicon nitride gate dielectric," *Appl. Phys. Lett.*, **90** (13), p. 133514, (2007).

6. K. S. Kim et al., "Large-scale pattern growth of graphene films for stretchable transparent electrodes.," *Nature*, **457** (7230), pp. 706-10, (2009).

7. T. Lohmann, K. V. Klitzing, and J. H. Smet, "Four-Terminal Magneto-Transport in Graphene p-n Junctions Created by Spatially Selective Doping" 2009," *Nano Lett.*, (2009).

8 M. Freitag *et al.*, "Energy Dissipation in Graphene Field-Effect Transistors," *Nano Lett.*, pp. 5-10, (2009).