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Wafer-scale Graphene Synthesis, Transfer and FETs

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Abstract — **Growth and characterization of graphene grown using copper foils as well as copper films on silicon dioxide on silicon substrates were performed. Kinetics of growth and effective activation energy for the graphene synthesis will be discussed for the surface catalytic synthesis of graphene. Conditions for large-scale synthesis of monolayer graphene will be addressed in this talk. Wafer-scale graphene transfer and electrical results will be presented. Based on our preliminary results from capped 100mm wafer scale graphene transistors, we expect a mobility of 4-6 k cm^2/Vs with symmetry hole/electron transport. Key considerations and challenges for scaling are discussed and results for graphene growth on the 300mm wafer scale will be discussed.**

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I. Introduction

To produce devices based upon graphene, three key steps are required: growth, transfer and device integration.

II. Graphene Growth

Growth of graphene was performed using catalytic decomposition of methane or ethylene on copper [1]. Using a vertical-flow, cold-wall reactor with short gas residence time (AIXTRON Black Magic), we were able to observe the early stages of growths to study the kinetics of the growth process and demonstrate uniform synthesis at wafer scale. In the first step, copper foils or wafers with a stack of 500 nm Cu on 150 nm SiO_2 were heated up to 925 ^oC (surface temperature) under a hydrogen atmosphere for 5 minutes. Under these conditions, the copper crystallises into a particular orientation, in particular for foil into <110> whereas on the SiO_2 wafer into <111> as verified by X-ray diffraction. After this step, hydrocarbon gas (methane or ethylene) is added to the gas flow which begins the growth process. To improve the quality of the graphene and suppress the formation of amorphous carbon, the growth step is normally performed under Ar dilution with the hydrogen flow reduced [2]. This two-step

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process is used to grow high quality, full coverage wafer-scale graphene as shown in Figure 1.

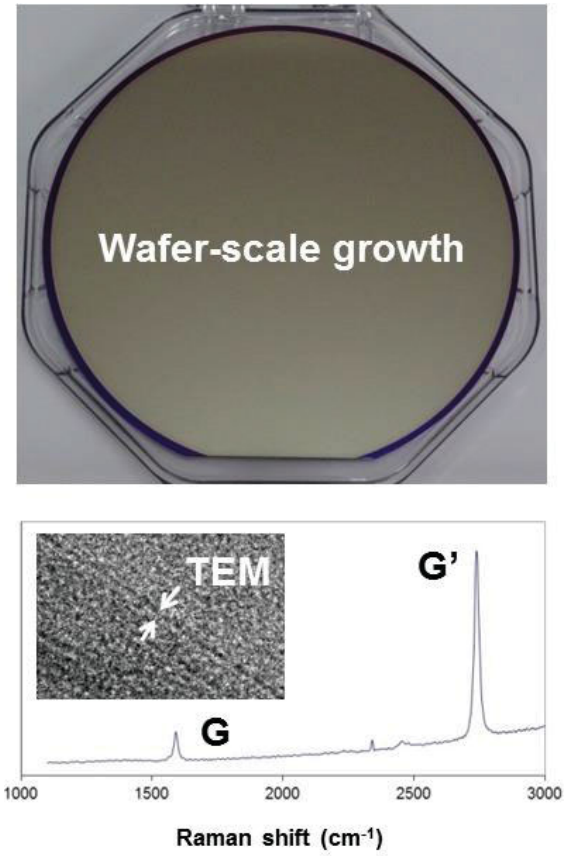

Figure 1: Graphene growth on Cu/SiO_2/Si wafer.

Next, we investigate the growth kinetics by varying the growth temperature, growth time to deliberately stop the film growth and measure the resultant graphene flake area as shown in Figure 2. The data is fitted by a modified Gompertz function; qualitatively, a sigmoidal increase in flake size can be observed by increasing the time and temperature. The sigmoidal growth curves implicate the existence of two distinct and disparate growth regimes, before and after the inflection points. The activation energy (E_A) is calculated by making an Arrhenius plot of the growth rate at the *inflection* points at each temperature (Figure 2, inset): 3.1 eV; this value corresponds well to the catalytic dehydrogenation of hydrocarbons on copper, which we suggest is the rate limiting step in the growth process.

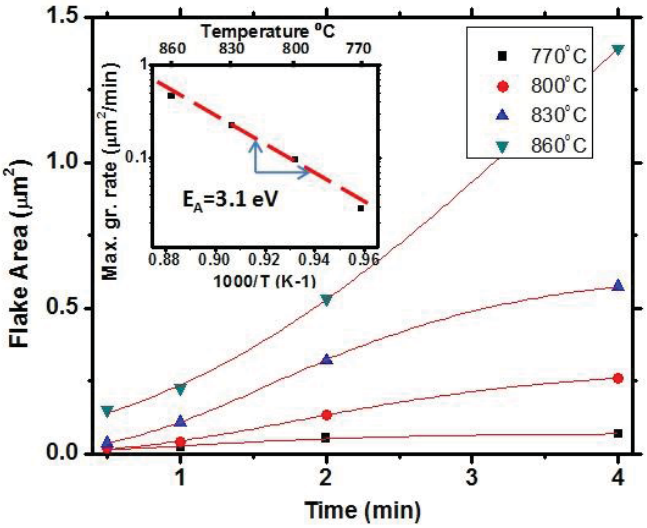

Figure 2: Growth kinetics of graphene flakes at different temperatures and time.

The increasing growth rate before the inflection point is believed to be caused by initial capture of C from the supersaturated surface forming the graphene growth front and the reduction of copper sublimation (which hinders growth) under the flake. After the inflection point, there is loss of exposed Cu surface for catalytic dehydrogenation of the hydrocarbon, leading to the observed reduction of the growth rate [3].

III. Graphene Transfer

Graphene is normally transferred using a sacrificial PMMA layer which is spun onto the graphene surface, copper etched, and then the graphene+PMMA transferred to a target wafer before finally dissolving away the PMMA. Here, we describe

a novel frame-assisted bubble transfer technique [4], as shown in Figure 3. Through electrolysis, hydrogen bubbles form at the graphene/copper interface which eventually delaminate the graphene from the copper.

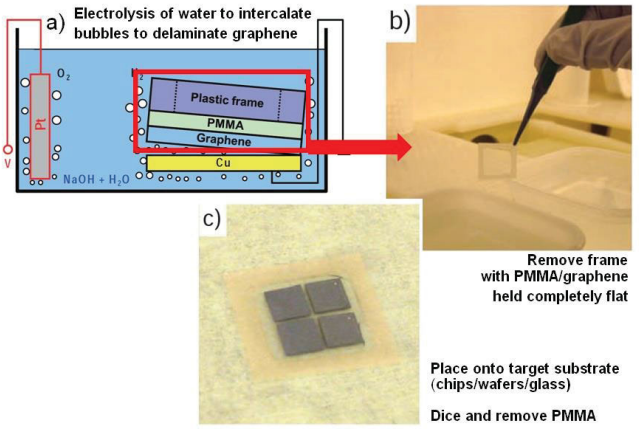

Figure 3: Frame-assisted electrolysis and transfer of graphene films.

The frame allows the graphene to be held flat throughout the transfer process, which minimises wrinkles, folds and defects in the transferred graphene. Another key advantage of this technique is that the copper is not etched away and so can be used again for growth. The recycling of the copper substrate ultimately drives down the total cost of graphene production.

IV. Graphene Devices

Grapehene was transferred onto silicon substrates with a 285 nm thick silicon dioxide layer. The graphene was then patterned into 3 µm wide and 21 µm long channel regions via photolithography and oxygen reactive ion etching. Titanium (2 nm) and palladium (48 nm) source/drain and four point contacts were then fabricated onto the graphene channels. The silicon substrate was used as the gate for our measurements. We measured a mobility of 4,000-6,000 cm^2/Vs with symmetry hole/electron transport.

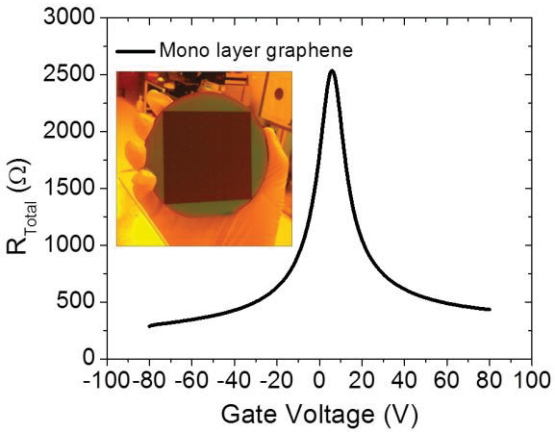

Figure 4: Electrical measurement of graphene FET

V. Conclusion

This work demonstrates the growth, transfer and integration of graphene resulting in a full fabrication workflow to achieve wafer-scale devices. Key considerations and challenges for scaling and results for graphene growth on the 300-mm wafer scale will also be shown during the presentation.

Acknowledgements

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REFERENCES

[1] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, Science, 324, 1312 (2009)

[2] L. Tao, J. Lee, H. Chou, M. Holt, R. Ruoff and D. Akinwande, ACS Nano 6, 2319 (2012)

[3] K. Celebi, M.T. Cole, J.W. Choi, F. Wyczisk, P. Legagneux, N. Rupesinghe, J. Robertson, K.B.K. Teo and H.G. Park, Nano Lett dx.doi.org/10.1021/nl303934v, to be published (2013)

[4] C.J. Lockhart de la Rosa, J. Sun, N. Lindvall, M.T. Cole, Y. Nam, M. Loffler, E. Olsson, K.B.K. Teo and A. Yurgens, Appl Phys Lett, 102, 022101 (2013).